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THE UNIVERSITY OF ALBERTA

INTERMODULATION DISTORTION ANALYSIS OF A MICROWAVE GaAs FET AMPLIFIER

by

©

RAMESH K. GUPTA

A THESIS
SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH
IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE
OF DOCTOR OF PHILOSOPHY

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THE UNIVERSITY OF ALBERTA

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research, for acceptance, a thesis entitled INTERMODULATION DISTORTION ANALYSIS OF A GaAs FET AMPLIFIER submitted by RAMESH K. GUPTA in partial fulfilment of the requirements for the degree of DOCTOR OF PHILOSOPHY.

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ABSTRACT

In this thesis, a mathematical model has been developed to predict the linear and nonlinear response of a microwave GaAs FET amplifier. The mathematical model is based on the Volterra-series representation of the amplifier input/output response. A 6 GHz microwave amplifier has been realised, using a GaAs FET device and microstrip circuits, in order to experimentally verify the predicted response.

A circuit model of the amplifier has been described that takes into account the device nonlinearities and their interaction with the surrounding microwave circuit. The surrounding microwave circuit is taken to consist of the matching circuits, the coaxial-to-microstrip transitions, and the discontinuities associated with the connectors and dc blocking capacitors. The nonlinearities within the device are estimated by least-square fitting the modeled device S-parameters to the measured two-port S-parameters. The nonlinear model for the amplifier has been used to analyze the third-order intermodulation distortion in the amplifier, for a two-tone equal amplitude input signal. The intermodulation distortion performance of the amplifier has been investigated as a function of microwave input signal level, signal frequency, and gate-bias on the device. Good agreement has been obtained between the measured and predicted results. The analysis has been extended to analyze the cross modulation distortion performance, gain compression and phase deviation of the amplifier, at increased input signal levels.

For the test device, the intermodulation distortion of the amplifier has been observed to decrease by approximately 6-dB for a -0.25V change in the gate-bias. A gate-bias compensation technique has been developed for improvement of the intermodulation distortion performance of the amplifier. Upto 10 dB improvement in distortion has been observed, over a limited range of input signal levels.

Up-conversion in the GaAs FET amplifier has been achieved by impressing an intermediate frequency (IF) signal on to the gate-terminal of the device. The Volterra-series model has been applied to the analysis of the up-conversion characteristics of the amplifier. Good agreement has been obtained between the measured and predicted results in the current saturation region of device operation. The up-conversion efficiency is observed to be a maximum in the pinch-off region of the device operation.

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LIST OF SYMBOLS

SYMBOL	DESCRIPTION
a	Device Epitaxial Layer Thickness.
$[A(j\omega)]$	Six-by-six system Matrix for the Overall Amplifier.
b	Width of the Conduction region in a FET.
b_p	Width of the Conduction region at Device Pinch-off.
b_x	Cross modulation Distortion Index.
b_1	The Modulation Index.
c	Velocity of Light.
C_{gs}	Gate-to-source Capacitance.
C_{dg}	Drain-to-Gate Capacitance.
C_o	Output Capacitance.
C_{gs_n}	nth Order Coefficient of Gate-to-Source Capacitance.
C_{dg_n}	nth Order Coefficient of Drain-to-Gate Capacitance.
$(CM)_F$	Cross modulation Factor.
$(CM)_A$	Amplitude Cross modulation Factor.
$(CM)_\phi$	Phase Cross modulation Factor.
C.C.	Complex Conjugate.
C_1, C_1'	Equivalent Capacitance of Coaxial-to-Microstrip Transitions.
d	Reduced Potential at the Drain.
E	Electric Field.
E_s	Saturation Electric Field.
E.F.	Error Function.

SYMBOL	DESCRIPTION
f	Frequency.
F_1, F_N	N Measurement Frequencies.
g_m	Transconductance of the Device.
g_{m_n}	nth Order Coefficient of Transconductance.
G_o	Inherent Device Gain.
G_s	Gain Contribution because of Source Matching of the Device.
G_L	Gain Contribution because of Load Matching of the Device.
G_T	Transducer Gain of the Amplifier.
h	Height of the Substrate.
$h_K(\tau_1, \tau_2, .., \tau_n)$	nth Order Volterra Kernel in Time Domain.
$H_K(\omega_1, \omega_2, .., \omega_n)$	nth Order Volterra Kernel in Frequency Domain.
$H(f_1-f_2)$	Ideal filter at f_1-f_2.
i^+	Forward component of the Equivalent Current.
i^-	Reverse component of the Equivalent Current.
$\hat{i}_{C_{gs}}$	Estimated Current due to Gate-to-Source Capacitance Nonlinearity.
$\hat{i}_{C_{dg}}$	Estimated Current due to Drain-to-Gate Capacitance Nonlinearity.
$\hat{i}_{g_m}$	Estimated Current due to Transconductance Nonlinearity.
I_d	Drain Current.
I_s, I_{dss}	Saturation Current.
$[I_{ni}(j\omega)]$	Input Current Vector.
IF	Intermediate Frequency.

SYMBOL	DESCRIPTION
IM_3	Third-order Intermodulation Distortion.
IM_5	Fifth-order Intermodulation Distortion.
K	Stability Factor.
ℓ, ℓ'	Equivalent Transmission Line Lengths in the Amplifier Model.
L	Device Gate Length.
L_d	Equivalent Drain Inductance.
L_g	Equivalent Gate Inductance.
L_s	Equivalent Source Inductance.
L_1, L_1'	Equivalent Inductance of Coaxial-to-Microstrip Transitions.
L_1	Length along the Device Channel at Pinch-off.
L_2	Length along the Device Channel beyond Pinch-off.
n_1, n_2	Frequency Dependent Transformer Ratios.
N	Number of Measurement Frequencies.
N_D	Doping Density
p	Reduced Potential at Device Pinch-off.
P_a	External Input Port of the Amplifier.
P_c	Connector Port of the Amplifier.
P_d	Device Port of the Amplifier.
P_{in}	Input Microwave Power.
P_o	Output Power at Fundamental Frequency.
P_I	Intercept Point.
q	Electronic Charge.
Q_a	External Output Port of the Amplifier.
Q_c	Connector Port of the Amplifier.

SYMBOL	DESCRIPTION
Q_d	Device Port of the Amplifier.
Q_o	Free Charge on the Gate Electrode.
R_d	Drain Resistance.
R_i	Charging Resistance.
R_s	Source Resistance.
R_o	Output Resistance.
S_{ij}	Scattering Parameters.
$S_{ij}^{(1)}$	Error Parameters at Port 1.
$S_{ij}^{(2)}$	Error Parameters at Port 2.
$S_{ij}^{(M)}$	Measured Scattering Parameters without Error Correction.
S_{ij_C}	Calculated Scattering Parameters.
S_{ij_M}	Measured Scattering Parameters.
t	Microstrip Substrate Thickness.
T_{F_1}, T_{R_1}	Forward and Reverse Transmission Coefficients.
v^+	Forward Component of the Equivalent Voltage.
v^-	Reverse Component of the Equivalent Voltage.
V_s	Saturation Velocity of Electrons.
V_{in}	Input RF Voltage.
V_{o_n}	nth Order Nodal Voltage Volterra Kernel at the Amplifier Output.
V_p	Pinch-off Voltage.
V_{IF}	IF Signal Voltage.
V_{fo}	Local Oscillator Signal Voltage.
V_{sg}	Source-to-Gate Voltage.
V_{sd}	Source-to-Drain Voltage.

SYMBOL	DESCRIPTION
V_{GS}	Gate-to-Source Bias Voltage.
V_{DS}	Drain-to-Source Bias Voltage.
V_{dd}	Drain Supply Voltage.
V_{gg}	Gate Supply Voltage.
Δw	Width Correction due to Finite Conductor Thickness.
$\Delta w'$	Width Correction due to Substrate Dielectric Constant.
W	Final Width of the Microstrip Conductor.
W'	Width of the Microstrip Conductor without Correction.
W_e	Effective Width of the Microstrip Conductor.
W_d	Depletion Layer Potential at the Drain.
W_p	Depletion Layer Potential at the Pinch-off.
W_s	Depletion Layer Potential at the Source.
W_{oo}	Gate-to-Channel Potential for Device Pinch-off.
W_1, W_2, W_3, W_4	Weighting Functions of the Error Function.
$x(t)$	Time-Domain Amplifier Input.
$X(\omega)$	Frequency-Domain Amplifier Input.
$y(t)$	Time-Domain Amplifier Output.
$Y(\omega)$	Frequency-Domain Amplifier Output.
y_{ω_n}	Amplifier Output at Frequency ω_n.
z	Device Width.
Z, Z'	Transmission Line Impedance in the Amplifier Equivalent Circuit Model.
$Z_s(\omega)$	Source Impedance as a Function of Frequency.
$Z_L(\omega)$	Load Impedance as a Function of Frequency.
Z_o	Characteristic Impedance.

SYMBOL	DESCRIPTION
$\bar{Z}(\omega)$	Normalised Impedance.
α,α'	Transmission Line Loss Factors in the Amplifier Equivalent Circuit Model.
α_c	Conductor Loss Coefficient.
α_d	Dielectric Loss Coefficient.
β_1,β_2	Arguments of Volterra Kernels.
Γ	Reflection Coefficient.
Γ_S,Γ_L	Source and Load Reflection Coefficients.
Γ_{in}	Input Reflection Coefficient.
$\Gamma_{in}^{(M)}$	Measured Input Reflection Coefficients.
Γ_{Fs},Γ_{Rs}	Forward and Reverse Reflection Coefficients with Short Circuits.
Γ_{Fm},Γ_{Rm}	Forward and Reverse Reflection Coefficients with Matched Terminations.
Γ_{Fo},Γ_{Ro}	Forward and Reverse Reflection Coefficients with Open Circuits.
ε_o	Free Space Permittivity.
ε_r	Relative Dielectric Constant.
ε_s	Permittivity of the GaAs Material.
$\varepsilon_e,\varepsilon_{eff}$	Effective Dielectric Constant.
η_{dB}	Up-Conversion Efficiency.
μ	Electron Mobility.
μ_o	Free Space Permeability.
ρ	Resistivity.
σ	Conductivity.
τ_o	Transit Time of the Electrons.
τ_1,τ_2,τ_3	Order Dependent Time Delays.
ϕ	Schottky-barrier Junction Potential.
ω	Radian Frequency.

CHAPTER I

INTRODUCTION

Intermodulation and cross modulation distortion of microwave amplifiers are important parameters for applications in multiple-carrier telecommunication systems. As input power level to an amplifier is increased spurious responses are generated within the amplifier band, thus degrading the performance. The third-order intermodulation product (IM_3) is of particular importance, since it lies nearest to the signal frequencies and generally dominates the distortion. The amplitude and phase response of the amplifier also show nonlinear characteristics, such as gain compression or expansion and phase deviation. These nonlinear characteristics result in transfer of modulation from one carrier to another for a frequency division multiplexed (FDM) input signal. The transfer of modulation among carriers is known as cross modulation distortion. Intermodulation and cross modulation distortion in microwave amplifiers arise because of nonlinearities associated with the electronic phenomena of the active device used for realising the amplifier. It is important, therefore, to understand these device nonlinearities and to develop suitable mathematical models to study the distortion performance of these amplifiers before they are put to use in telecommunication systems.

In recent years, Gallium Arsenide (GaAs) MEtal Semiconductor Field-Effect Transistors (MESFET) [1] have demonstrated superior performance characteristics as compared to other microwave solid-state devices, such as IMPATT and GUNN diodes and bipolar transistors. They have demonstrated high gain, higher power amplification efficiency, large bandwidths, and low noise-figure at X-band and higher frequencies in the microwave range. X-band GaAs FET amplifiers with power capabilities of 30 dBm and a small-signal gain of 13 dB have been reported [1]. Multioctave bandwidth amplifiers have been realised [2] and the design of a broad-band amplifier with minimum noise-figure of 2.2 dB has recently been reported [3]. Significant improvements in noise performance have been obtained by cooling the amplifiers. A 1.6 dB noise figure was measured at 60°K by Liechti and Larrick [4]. Because of these superior performance characteristics, GaAs FET devices may be used in the near future to replace microwave solid-state devices and Travelling-Wave Tube (TWT) amplifiers in satellite communication links and radar systems.

Recent trends in MESFET research have indicated their use for applications such as mixers [5], down-converters [6] and frequency multipliers [7]. Further analog applications such as modulators and up-converters are proposed. All these applications require an understanding of the device nonlinearities and their interaction with the microwave circuit surrounding them. Mathematical models that can be used to predict the nonlinear behavior of GaAs FETs are therefore of great interest to microwave design engineers.

---

[1] The terms GaAs MESFET, GaAs FET, MESFET and FET will be used interchangeably during the discussion in this thesis. Unless mentioned otherwise, all these terms are meant to represent a GaAs Schottky-Barrier gate Field-Effect Transistor

Significant developments have taken place in microstrip technology over the last two decades. Microstrip circuits are particularly suitable for use with microwave solid-state devices. Integrated GaAs FET amplifiers with microstrip circuits result in considerable savings in size, weight and cost. In order to design and realise integrated GaAs FET amplifiers with minimum circuit tuning, accurate characterisation procedures are essential. The use of computer aided design (CAD) techniques allows simulation of the amplifier response before the amplifier is actually fabricated. In this thesis, an approach is described for the accurate characterisation of a GaAs FET device. A 6 GHz integrated GaAs FET amplifier has been designed, realised and modeled using a CAD program. A nonlinear model has been derived from computer reduction of measured device data, and the nonlinear performance of the amplifier has been predicted.

1.1 Historical Background

Field-Effect Transistors using p-n junctions were first developed at Bell Labs. by Shockley [8] in 1952. It was recognised by Shockley that FET performance would be more efficient at higher frequencies as compared to that of bipolar transistors. The GaAs FET with Schottky-barrier gate was proposed by Mead [9] for microwave frequency applications. Gallium Arsenide is particularly suitable at high frequencies because the mobility of electrons is approximately six times greater in GaAs than in silicon. This results in a larger transconductance in GaAs FETs, a shorter transit time of electrons in the channel and a smaller channel resistance. Another significant factor contributing towards appications of GaAs FETs at microwave frequencies has been the technological improvement in producing micron- and submicron-length gates. The reduction of gate length reduces the gate capacitance, increases the maximum frequency of oscillation f_{max} . increases the device transconductance and reduces the noise figure. In 1970, first results of a 1 micron GaAs FET with an f_{max} of 50 GHz and an useful gain upto 18 GHz were published [10],[11]. The first X-band amplifiers with GaAs MESFETs were demonstrated in 1972 [12], [13]. Subsequent research focussed on developing better devices with higher f_{max}, better characterisation procedures, synthesis of input and output matching circuits to realise very broad-band amplifiers

[14], and increasing use of computer aided design programs [15], [16]. An excellent review of the developments in GaAs FETs up to 1976 with an extensive biblography is available in the literature [17].

In recent years, because of the large dynamic range and low noise properties of GaAs FETs, the nonlinear phenomena associated with the device is being exploited for system applications such as mixers, frequency converters and multipliers. Different analytical approaches have been suggested by various workers for nonlinear analysis of GaAs FET devices. These approaches are based on three distinct modeling philosophies; they are: a) Device physics approach, b) Quasi-linear analysis approach, and c)Frequency-domain analysis approach.

The device physics approach is basic to the physical operation of the device. It consists of obtaining a solution of the charge transport equations for prescribed boundary conditions [8],[18]. The approach has been extended for nonlinear analysis by Madjar and Rosenbaum [19]. The results are related to the physical parameters of the device such as device dimensions, doping density and doping profiles. The approach is very useful for the understanding of device operation, but requires extensive computer time and is inconvenient for an engineer or designer to use.

The quasi-linear approach for distortion analysis of a GaAs FET has been developed by Willing et al. [20] and is based on circuit characterisation of the device. The nonlinear intrinsic elements within the device are expressed as a function of gate-to-source voltage V_{GS}, and drain-to-source voltage V_{DS}. A numerical method is used to find time-domain voltage and current waveforms within the device, which are then Fourier analyzed for various frequency components. This approach normally requires a large amount of computer time. Furthermore, the frequency dependence of distortion can not be conveniently modeled.

The third approach has been developed by Gupta et al.[21] and uses a frequency-domain analysis based on the Volterra-series expansion of the overall response of the amplifier. This approach will be the topic of extensive discussion in this thesis. The Volterra-series approach is useful in that the response can be modeled for systems with memory (reactive) elements and therefore the frequency dependence of the nonlinear response can be obtained. This approach is useful for mild nonlinearities. The complexity of the analysis rapidly increases if large nonlinearities are encountered .

1.2 Thesis Objectives

The objective of this thesis is to develop a mathematical model for a GaAs FET amplifier so that the linear and nonlinear performance of the amplifier can be analyzed. The following performance characteristics are studied:

a) Gain and phase response of the amplifier and their dependence on frequency, as well as the dependence of the amplifier gain and bandwidth on the transistor biasing conditions.

b) The intermodulation distortion for a two-tone input signal and its dependence on the input power level and the frequency of the two tones, as well as the gate-bias of the transistor.

c) Analysis of crossmodulation distortion and computation of AM-to-AM and AM-to-PM conversion.

d) Gain compression and phase deviation of the amplifier with increasing input signal.

f) Up-conversion characteristics of a single gate MESFET amplifier up-converter. The up-conversion is achieved by impressing an IF signal onto the gate terminal of the amplifier.

The mathematical model of the amplifier can be obtained by circuit characterisation and circuit modeling of the amplifier. The accuracy of mathematical models for analysis of the amplifier response is dependent on the accuracy of the device characterisation. Therefore, in order to meet the main objective of the thesis, the following additional objectives were established:

a) An accurate characterisation procedure for the device and the microwave circuit must be developed. The nonlinearities associated with the intrinsic elements of the device can be estimated from the measured device S-parameters at various gate and drain potentials.

b) A 6 GHz stable microwave amplifier using a GaAs FET device and a microstrip circuit must be designed and realised.

c) A distributed and lumped circuit model for the amplifier must be established. The circuit model should be able to take into account the interaction of the active device with the surrounding microwave circuit.

1.3 Thesis Organisation

In chapter II, the equations for the nonlinear intrinsic elements within a FET are derived from a device physics model and their relevance with further work in this thesis is discussed. Basic microstrip concepts are reviewed and the relationship between the physical constants of the microstrip such as width of the microstrip, height and dielectric constant of the substrate and electrical parameters, such as the characteristic impedance and guide wavelength, are discussed.

In Chapter III, a characterisation methodology is developed for accurate modeling of the device and the circuit. The characterisation procedure features in-situ characterisation of the device and combines network analyzer measurements with CAD programs to realise accurate models.

In chapter IV, results from an actual amplifier are summarised. The difficulties involved with the actual realisation of the GaAs FET amplifier, biasing considerations and stability problems are discussed.

In chapter V, a lumped circuit amplifier model is described and is used to develop a mathematical Volterra-series analysis model. The model is used for analysis of intermodulation and cross modulation distortion and comparison is made with measured results.

In chapter VI, a method is described for achieving upconversion in single-gate MESFET amplifiers. A model is described for analysis of the up-conversion characteristics of the amplifier and comparison is made with experimental results.

In Chapter VII, the important conclusions of this research are summarised and some recommendations are made for further research.

CHAPTER II

REVIEW OF GaAs FET DEVICE PHYSICS AND MICROSTRIP CHARACTERISTICS

In this chapter, GaAs FET and microstrip concepts are reviewed. The significant technological factors influencing the performance of microwave GaAs FETs are discussed. The intrinsic device elements and their relationships with physical device parameters are discussed. These relationships form the basis for further nonlinear modeling of the device.

Microstrip concepts are reviewed, with particular emphasis on those parameters that are relevant to the work in this thesis. The factors influencing the choice of the microstrip dielectric constant (ε_r) and substrate thickness are explained. Relationships are described for the computation of the characteristic impedance and losses associated with the microstrip.

2.1 Introduction

The principle of operation of a p-n junction Field-Effect Transistor was first described by Shockley in 1952 [8]. Since then there has been a continuous effort to develop devices capable of amplification and oscillations at higher frequencies. Gallium Arsenide FETs, in particular, have superior performance characteristics at microwave frequencies because of the low resistivity of GaAs, the higher carrier velocity and small transit times. Based on the assumption that the field distribution below the gate in a FET can be treated as a superpostion of two one-dimensional fields, Shockley carried out an initial analysis of a FET using basic device physics. His analysis has formed the basis for almost all subsequent analyses carried out from a device physics point of view. Various modifications of Shockley's original theory have been reported and an excellent review of these developments is available in the literature[22]. Recent studies on GaAs FETs were directed towards arriving at the optimum device dimensions and physical parameters for obtaining the best performance from GaAs FETs[3],[18],[23]. Some of the conclusions from these studies are discussed in the following section.

2.2 Some Technological Features of Microwave GaAs FETs

The following technological developments have contributed largely towards the successful use of GaAs FETs at microwave frequencies.

a) Larger transconductance, smaller parasitic resistance and shorter transit times of electrons are obtained by the use of Gallium Arsenide as a substrate material for FETs. The conduction electrons in GaAs have a mobility six times greater and a peak velocity two times larger than conduction electrons in silicon.

b) The active layer is grown on a semi-insulating GaAs substrate with a resistivity greater than 10^8 ohm-cm. The parasitic reactances at the gate and drain are reduced by positioning the pads on the substrate.

c) Reduction of gate length results in smaller gate capacitances, large transconductance and shorter transit times.

The overall performance of GaAs FETs is a function of the geometrical and material parameters of these devices. These parameters are listed in Table 2.1. An increase in the doping density N_D results in a larger transconductance, larger gate capacitance and increased noise-figure. Devices with a large epitaxial layer thickness show very good gain properties; the noise figure of such devices is, however, degraded. In a recent study by Fukui [3], semi-empirical expressions for the transconductance g_m, gate-to-source capacitance C_{gs}, and cut-off frequency have been suggested. It has been shown that g_m is inversely related to gate-length L, whereas C_{gs} varies as square of L. The cut-off frequency therefore increases in inverse proportion to the gate-length L. The device width Z is an important parameter influencing the power handling capabilities of the device. A larger device width results in larger power handling capacity and larger C_{gs} in the device.

TABLE 2.1

1. n-type GaAs FET Material Constants

Parameter	Symbol	Typical Room Temperature Value
Mobility	μ	$4700 cm^2 V^{-1} S^{-1}$
Doping Density	N_D	$1 \times 10^{17} cm^{-3}$
Resistivity	ρ	1.33×10^{-12} ohm-cm
Conductivity	σ	75.2×10^{10} mho-cm^{-1}
Saturation Velocity	V_s	$1.67 \times 10^7 cms^{-1}$
Saturation Field	E_s	$3945 V cm^{-1}$
Dielectric Constant	ε_r	12.5
Permittivity	$\varepsilon_s = \varepsilon_r \varepsilon_o$	1.107×10^{-12} F-cm^{-1}

2. FET Structure

Parameter	Symbol	Value for FET
Epitaxial layer thickness	a	0.2 ± 0.04 μm
Interelectrode Spacing:		
Source-to-Gate	L_s	1μm
Gate-to-Drain	L_d	2μm
Gate Length	L	1μm
Device Width	Z	500μm

2.3 DC Analysis and Small-signal Theory:

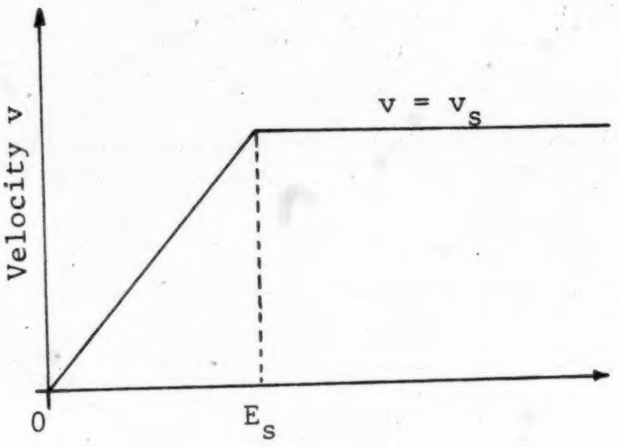
The analysis of FETs involves solution of the device physics relations within prescribed boundary conditions. Such investigations have been the topic of a large number of papers. The analysis described by Pucel et al.[22] will be reviewed here so as to describe the basic device operation and to derive relationships for intrinsic elements. A number of assumptions are involved in the analysis, some of which will be described here. Reference should be made to figure 2.1(a) and 2.1(b).

Assumption I:

The cross section of the channel varies slowly as one moves from source to drain. This assumption is called the Gradual Channel Approximation (GCA). Such an assumption holds if the gate length L is approximately three or more times the channel thickness dimension 'a'. Typically, X-band GaAs FETs have a gate length of 1 μm and a channel thickness 'a' of 0.3 μm. Therefore the GCA approximation is a valid assumption for the analysis.

Assumption II:

The velocity-field characteristics of GaAs are assumed to be piece-wise linear. The GaAs FET channel is divided into two regions. In region I, the mobility of electrons in the channel is assumed constant. In region II, the mobility of the carriers is assumed field-dependent such that the



Electric Field E

Fig. 2.1(a) Piecewise Linear Approximation of Electron Velocity vs. Electric Field Characteristic in a GaAs FET

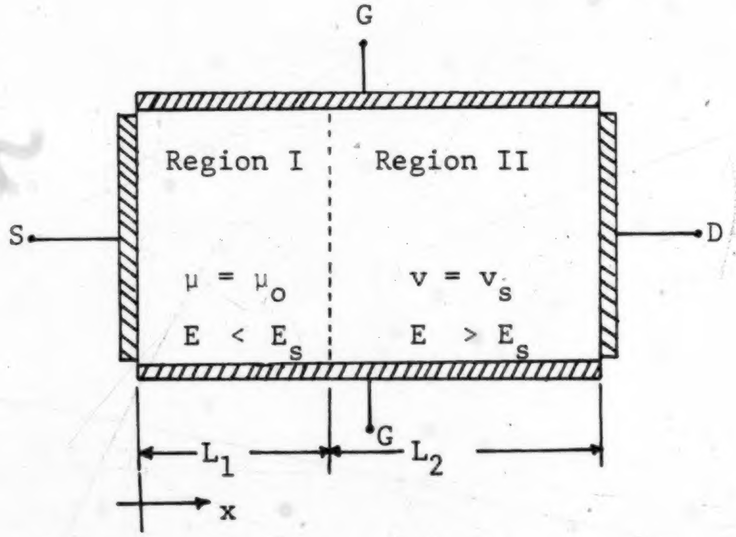

G
Region I
Region II
S
D
$\mu = \mu_o$
$v = v_s$
$E < E_s$
$E > E_s$
G
L_1
L_2
x

Fig. 2.1(b) Two-Section Model of the FET Based on the Velocity-Field Characteristic of Fig. 2.1(a) carrier velocity is saturated. L_1 defines the length along the channel defining the onset of pinch-off.

Assumption III:

The space charge region lies entirely in the channel. That is, the width of space charge region in the gate is negligible. Such an assumption is valid in MESFETs since the junction is formed between metal and a semiconductor.

Assumption IV:

The conducting channel height $2b_p$ in region II is assumed to be constant and equal to the channel height at the pinch-off point ($x=L_1$).

The longitudinal electric field distribution and the potential distribution along the FET channel are shown in Fig. 2.2. The gate and drain potentials referred to the source can be denoted by V_{sg} and V_{sd}, respectively. The potential at a distance x from the source is $V(x)$ and its value at pinch-off point $x=L_1$ is denoted by $V = V(L_1)$. The potential at point x in the depletion region is denoted by, $W(x)$. Thus

$$W(x) = V_{sg} + \phi - V(x) \qquad (2.1)$$

ϕ is the 'built-in' potential of the gate junction, and is typically 0.8V for GaAs Schottky-barrier junctions. The

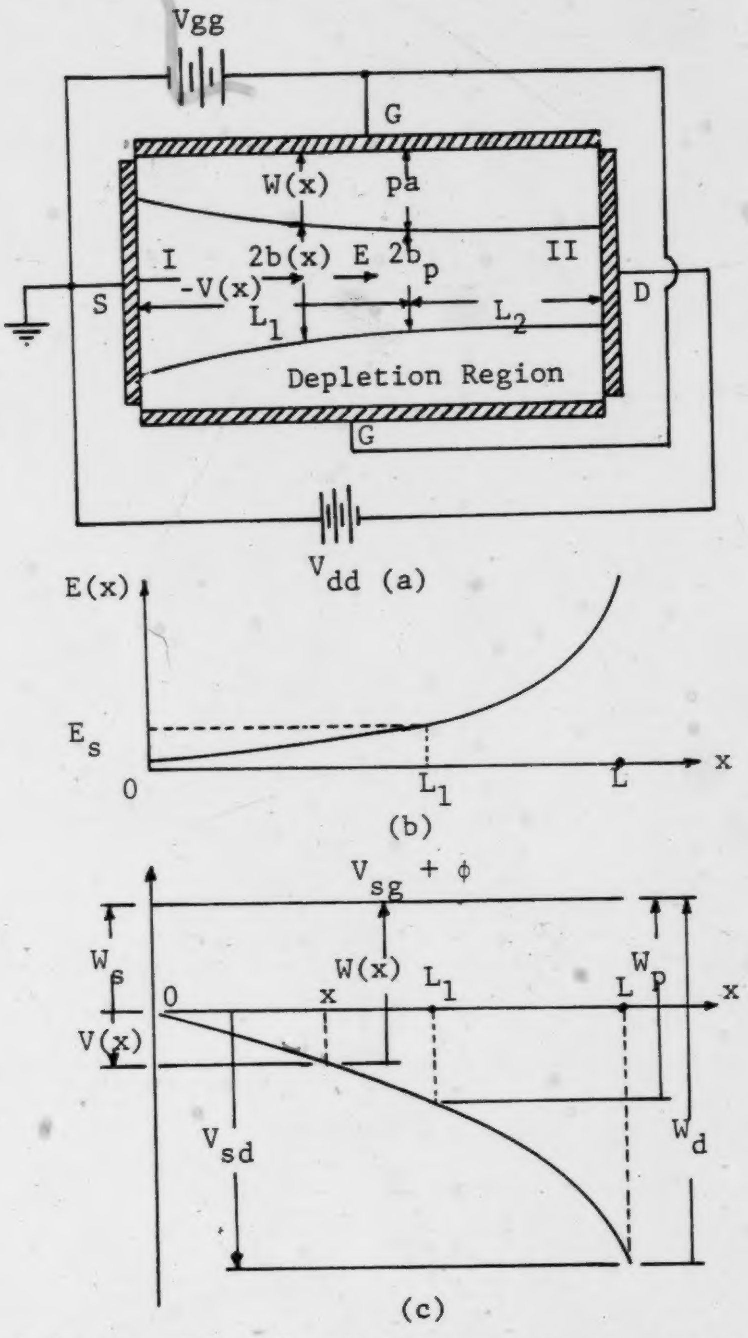

Vgg
G
W(x)
pa
I
2b(x)
E
$2b_p$
II
S
-V(x)
L_1
L_2
D
Depletion Region
G
V_{dd}
(a)
E(x)
E_s
0
L_1
L
x
(b)
$V_{sg} + \phi$
W_s
0
x
W(x)
L_1
L
W_p
x
V(x)
V_{sd}
W_d
(c)

Fig. 2.2 Cross-Sectional Diagram of the Idealized FET

(a) Bias Voltages, Channel Dimensions, and Reduced Potentials

(b) Electric Field Distribution Along Source-to-Drain Plane of Channel

(c) Potential Distribution Along Source-to Drain Plane of the Device following depletion layer potentials can be defined

$W_s = V_{sg} + \phi$ (2.2 a)

$W_p = V_{sg} + \phi - V_p$ (2.2 b)

$W_d = V_{sd} + \phi - V_p$ (2.2 c)

where W_s , W_p and W_d are the values of W(x) at source, drain end and the pinch-off plane.

The following reduced potentials are introduced so as to simplify the analysis.

$s = (W_s/W_{oo})^{\frac{1}{2}}$ (2.3)

$p = (W_p/W_{oo})^{\frac{1}{2}}$ (2.4)

$d = (W_d/W_{oo})^{\frac{1}{2}}$ (2.5)

$w(x) = (W(x)/W_{oo})^{\frac{1}{2}}$ (2.6)

where, W_{oo} is the gate-to-channel potential required to deplete the channel completely of the carriers and represents the 'pinch-off' voltage for the Shockley model. W_{oo} is given by

$W_{oo} = (q\ N_D/2.\varepsilon_s)a^2$ (2.7)

where 'a' is half the thickness of the semiconductor between the gate electrodes, q is the electronic charge, N_D is the doping density and ε_s is the dielectric constant of

GaAs.

Because of the drain current, there is a potential drop along the channel. As the drain electrode is approached, the depletion region between gate and source widens and the channel is constricted. Using the Gradual Channel Approximation, the channel-to-gate potential $W(x)$ is obtained by integration of the one-dimensional Poisson's equation in the y-direction in the depletion region. $W(x)$ is given by

$$W(x) = W_{oo}\,(1 - b(x)/_{a})^{2} \qquad (2.8)$$

In region I of constant mobility, the drain current is given by Ohm's law.

$$I_d = 2b(x)\ Z\sigma\ (\partial W/_{\partial x}) \qquad (2.9)$$

The symbols and their dimensions are explained in Table 2.1 and Figure 2.2.

Integration of above equation from 0 to L_1, gives the drain current in terms of reduced potentials.

$$I_d = \frac{g_o Z W_{oo}}{L_1}\, f_1(s,p) \qquad (2.10)$$

where

$$f_1(s,p) = p^2 - s^2 - 2/_3(p^2 - s^2) \qquad (2.11)$$

and $g_o = 2a\sigma$

for a symmetric FET.

For asymmetric channels, the factor 2 from the above expression should be dropped.

In region II, where the electrons move with constant saturated velocity V_s, the drain current is given by

$$V_s = \mu_o E_s \qquad (2.12)$$

$$I_d = g_o Z E_s \; (1-p) \qquad (2.13)$$

Comparing (2.10) and (2.13) it is possible to find an expression for length L_1 along the channel, where pinch-off sets in. In addition the following expression for source to drain potential has been derived[22].

$$V_{sd} = -W_{oo} \left[(p^2 - s^2) + \frac{2}{\pi} \left(\frac{aE_s}{W_{oo}} \right) \text{Sinh} \; \frac{\pi L_2}{2a} \right] \qquad (2.14)$$

These expressions for drain current and the source-to-drain potential are used in the next section to compute expressions for small-signal parameters in the intrinsic device.

2.4 Small-signal Parameters:

An equivalent circuit of the device is shown in Fig.2.3. The figure depicts the location of various circuit elements within the device. The equivalent circuit consists of three regions; the intrinsic parameters associated with basic electronic device phenomena, the extrinsic parameters

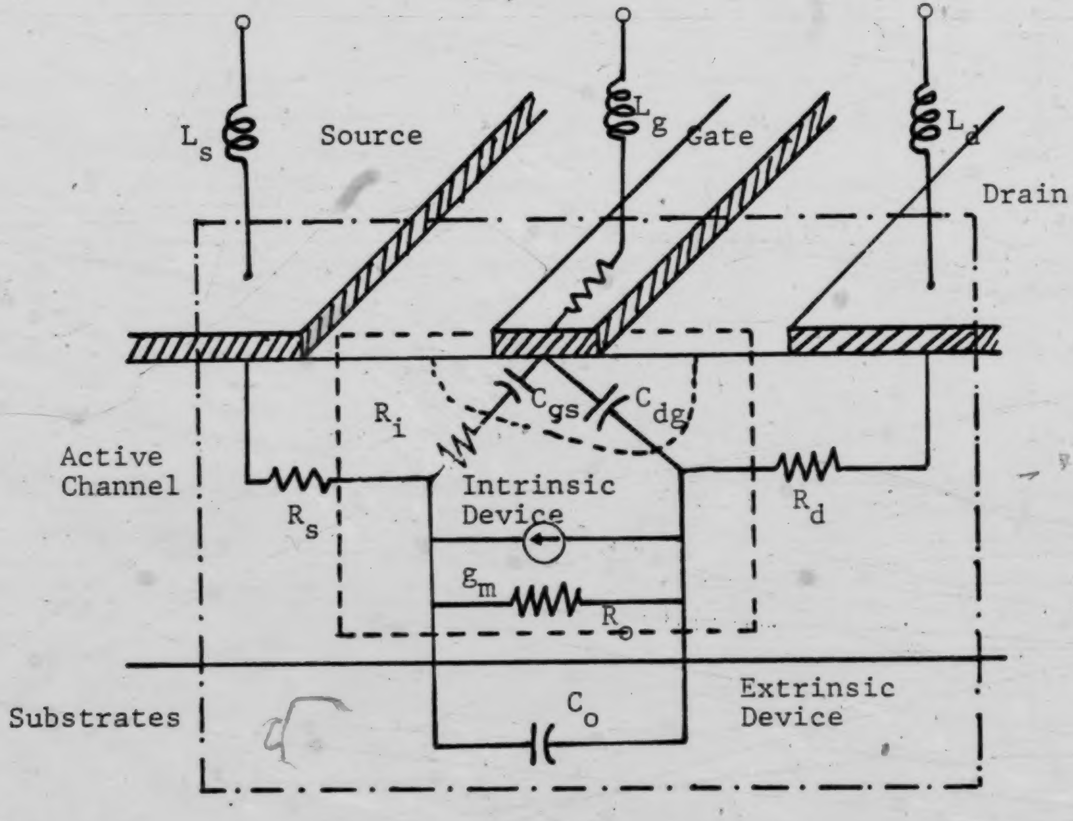

L_s
Source
L_g
Gate
L_d
Drain
R_i
C_{gs}
C_{dg}
Active Channel
R_s
Intrinsic Device
g_m
R_o
R_d
Substrates
C_o
Extrinsic Device

Fig. 2.3 An Equivalent Circuit of the GaAs FET Device. The Origin of Equivalent Circuit Elements Within the Device is Shown

associated with the active device channel and the substrate and the package reactances originating from the device packaging. The circuit elements within the intrinsic device are nonlinear functions of the device potentials; these five nonlinear elements are the gate-to-source capacitance C_{gs}, the drain-to-gate capacitance C_{dg}, the transconductance g_m, the output resistance R_o, and the charging resistance R_i. Resistance R_i is almost linear and the capacitance C_{dg} displays relatively mild dependence on the applied gate potential. The transconductance g_m and gate capacitance C_{gs} are basic to the gain mechanism of the device and are dependent on gate-voltage. The output resistance R_o is dependent on the drain-to-source voltage, V_{DS}.

2.4.1 Intrinsic Elements:

1. Transconductance g_m:

In the current saturation region of device operation, the transconductance of the device can be obtained from (2.12), by computing the small change in drain current produced by a small change in gate voltage, when the drain voltage is kept constant; g_m is given by

$$g_m = -\partial I_d/\partial V_{sg} \Big|_{V_{sd} = \text{constant}} \qquad (2.15)$$

$$= (g_o E_s Z/2sW_{oo})\, \partial p/_{\partial s} \qquad (2.16)$$

For short gate-length devices, it can be assumed that $s \approx p$. Such an assumption is valid, since for a device with a gate-length of 1 m and channel thickness $a = 0.3$ μm, region II encompasses 96% of region under the channel for large source-to-drain voltage V_{DS}. The expressions for g_m can be simplified to

$$g_m = I_s/W_{oo} \frac{1}{2p} \qquad (2.17)$$

$$= I_s'/2W_{oo}\left(\frac{1}{I - I_{d/I_s}}\right) \qquad (2.18)$$

$$= I_s/_{2W_{oo}}\left(1 - \left(\frac{Vsg + \phi}{W_{oo}}\right)^{\frac{1}{2}}\right) \qquad (2.19)$$

Such an expression holds in the current saturation region of device operation ($I_d/I_s > 0.1$).

2. Output Resistance R_o:

The Output resistance in the saturation region can be computed from (2.13) and (2.14), by calculating the small change in drain-to-source potential corresponding to a small change in drain current. R_o is defined as

$$R_o = \left.\frac{-\partial V_{sd}}{\partial I_d}\right|_{Vsg\, =\, \text{constant}} \qquad (2.20)$$

For short gate-lengths and drain currents in the operating region of interest, the expression for R_o simplifies to

$$R_o = \frac{\pi W_{oo}}{E_s a} \frac{|V_{sd}|}{I_d} p \qquad (2.21)$$

R_o is linearly dependent on the source-to-drain potential and the gate-length. It may be pointed out, however, that in practical devices the output resistance is usually lower than the computed value and may be an arbitrary function of operating potentials because of leakage paths on the the surface or through the substrate.

3. Gate-to-Source Capacitance C_{gs}:

The gate-source capacitance C_{gs} can be defined as the rate of change of free charge on the gate electrode with respect to gate bias voltage when the drain potential is held fixed.

$$C_{gs} = \left.\frac{\partial Q_o}{\partial V_{sg}}\right|_{V_{sd} = \text{constant}} \qquad (2.22)$$

For short gate-lengths, using $s \simeq p$, and $L_1 \simeq 0$, the expression for C_{gs} can be simplified to a considerable degree

$$C_{gs} \simeq 2\varepsilon_s Z \left[\frac{L}{ap} + 1.56\right] \qquad (2.23)$$

$$= 2\varepsilon_s Z \left[\frac{L}{a}\left(1 - \left(\frac{V_{sg} + \phi}{W_{oo}}\right)^{\frac{1}{2}}\right) + 1.56\right] \qquad (2.24)$$

C_{gs} is a function of source-gate potential V_{sg}, and is approximately linearly dependent on the gate-length.

4. Drain-Gate Capacitance C_{dg}:

C_{dg} is largely a parasitic capacitance within the device. Therefore, it shows small dependence on the gate voltage. Because of its being a feedback Miller Capacitance, it is important to include it in the device equivalent circuit.

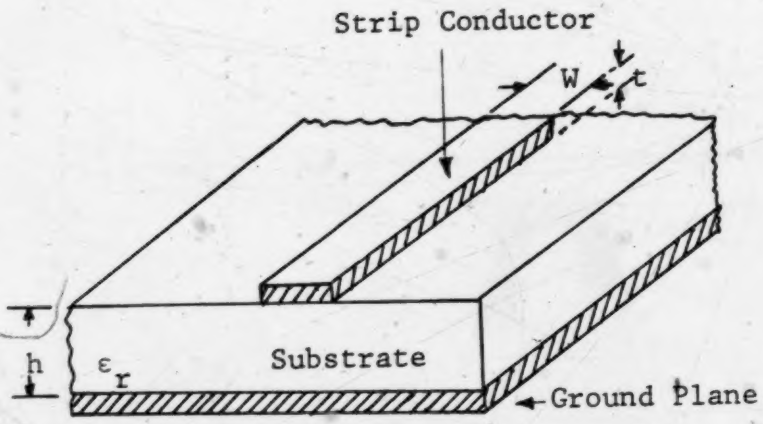
2.4.2 Extrinsic and Package Parameters:

The extrinsic resistances in the drain, gate and source terminals arise because of interfacial contact resistances at the terminals and the bulk resistance of the active channel. These resistances do not influence the intrinsic small-signal device behavior but strongly affect the noise performance of the FET. The drain resistance R_d is usually larger than the source resistance because of larger interelectrode spacing in the drain circuit. The capacitance in the drain circuit depends on the device dimensions and is usually of the order of 0.1 to 0.5 pF. In the equivalent circuit shown in Figure 2.3, the capacitance in the drain circuit has been returned to the source resistance instead of source contact terminal. This has been done to simplify the equivalent circuit.

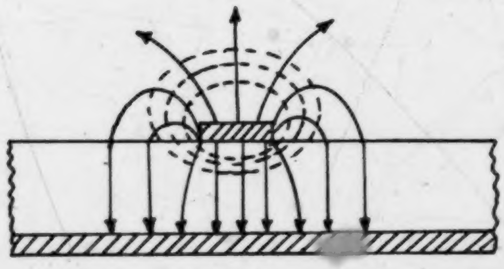
The packaging of the device further introduces package parasitic rectances. Typically, these parasitics can be modeled in the form of inductors of value less than 1nH and fringing capacitances of up to 0.3 to 1.0 pF. These package parasitics strongly influence the frequency response of the device, particularly when the device is operated towards the higher end of the microwave frequency range. In order to realise broadband amplifiers these parasitics must be kept as small as possible.

2.5 Microwave Integrated Circuits and Microstrips:

In recent years, significant developments have taken place in microstrip and stripline technology along with developments in microwave solid-state devices. The culmination of these two technologies has resulted in the realisation of microwave integrated circuits, thus decreasing the size and cost of microwave amplifiers with increased reliability and reproduceability. Stripline consists of a narrow conductor sandwiched between two dielectric layers shielded by ground planes. In comparison, the microstrip has only half shielding, that is it consists of a strip conductor separated from a ground plane by a dielectric on one side and air on the other side. The half shielding is adequate for most practical purposes, because the external field is relatively weak. Microstrip configuration and its electric and magnetic fields are shown in Fig. 2.4. The open microstrip configuration has added advantage over striplines in that it offers added convenience in circuit tuning and results in circuits with


Strip Conductor
W
t
h
ε r
Substrate
Ground Plane

(a) Isometric View



(b) Front View

Electric Field
Magnetic Field

Fig. 2.4 Basic Microstrip Configuration

smaller weight and volume.

In a microstrip the field lines between the conductor strip and the ground plane are not confined entirely in the substrate; therefore the propagating mode along the strip is not purely transverse electromagnetic (TEM). Because of the external fields along the microstrip, the effective dielectric constant of the microstrip ε_e is lower than relative dielectric constant ε_r of the substrate. The phase velocity in microstrip is given by

$$v_p = c/\sqrt{\varepsilon_e} \qquad (2.25)$$

where c is the velocity of light.

A number of papers describe the performance of microstrip line based on a quasi-TEM model. The quasi-TEM approximation remains valid at lower frequencies in the microwave range; at higher frequencies, hybrid-mode models of microstrips are used to calculate the line impedance. Accurate empirical relations for the computation of microstrip impedance has recently been described by Wheeler [24]. These formulas are valid for a large range of strip conductor widths and dielectric constants ε_r, within an accuracy of 1%. For the assumption that the thickness of strip conductor is zero (t=0), Wheeler has suggested the following relationships.

For a required characteristic impedance the width to height ratio of a microstrip, for a given substarte, can be computed from the following relationship

$$W'/_h = \frac{8\sqrt{\exp\left(Z_o/42.4 \cdot \sqrt{\varepsilon_r + 1}\right) - 1 \quad \frac{7 + 4/\varepsilon_r}{11} + \frac{1 + 1/\varepsilon_r}{0.81}}}{\left[\exp\left(Z_o/42.4 \sqrt{\varepsilon_r + 1}\right) - 1\right]} \tag{2.26}$$

and the following inverse relationship can be used to compute the characteristic impedance of a microstrip, for a given width to height ratio

$$Z_o = \frac{42.4}{\sqrt{\varepsilon_r + 1}} \ln\left\{1 + \left(\frac{4h}{W'}\right)\left[\left(\frac{14 + 8/\varepsilon_r}{11}\right)\left(\frac{4h}{W'}\right) + \sqrt{\left(\frac{4 + 8/\varepsilon_r}{11}\right)^2 \left(\frac{4h}{W'}\right)^2 + \frac{1 + 1/\varepsilon_r}{2}\pi^2}\right]\right\} \tag{2.27}$$

The effect of finite thickness of the conductor can be expressed in terms of width correction by use of relationships

$$\Delta w = 1/_\pi \ln \frac{4e}{\sqrt{(t/_h)^2 + \left(\frac{1/\pi}{W'/_t - 0.26}\right)^2}} \tag{2.28}$$

This effect of strip thickness, however, assumes that the dielectric constant of the substrate medium is 1. A further width adjustment has therefore been suggested [24]. The modified correction value is obtained from the following width correction

$$\Delta w' = \frac{1 + 1/\varepsilon_r}{2} \Delta w \tag{2.29}$$

and $W = W' - \Delta w'$ (2.30)

Using (2.26), and (2.28) to (2.30) the required width of a microstrip line can be computed for a prescribed impedance. Such computations were made for two substrate materials and the results are plotted in figure 2.5.

For large dielectric constant, the line width required is much smaller compared with that required for material with a lower dielectric constant. Therefore, low dielectric constant materials require physically large matching networks, resulting in larger size. Furthermore, they cause impedance discontinuities because the device leads are of much smaller size. From these considerations Epsilam-10 material with a dielectric constant of 10.2 was chosen. An added advantage of using this material is that it is reasonably flexible, so that it can be easily cut and handled. However, for realising high impedance lines, the line widths required are extremely thin. Therefore, a very high precision etching procedure is required for realising continuous lines of acceptable tolerances. Such an etching procedure was developed in our laboratory. The impedance of the line is dependent on the width to height ratio of the microstrip substrate. The thicker materials (larger h) require larger widths compared to the thinner substrates.

A metallic enclosure is required for most microwave integrated circuits for strength, electromagnetic shielding, and ease of handling. The top and side walls of the enclosure tend to lower the impedance and effective dielectric constant of the microstrip because the field

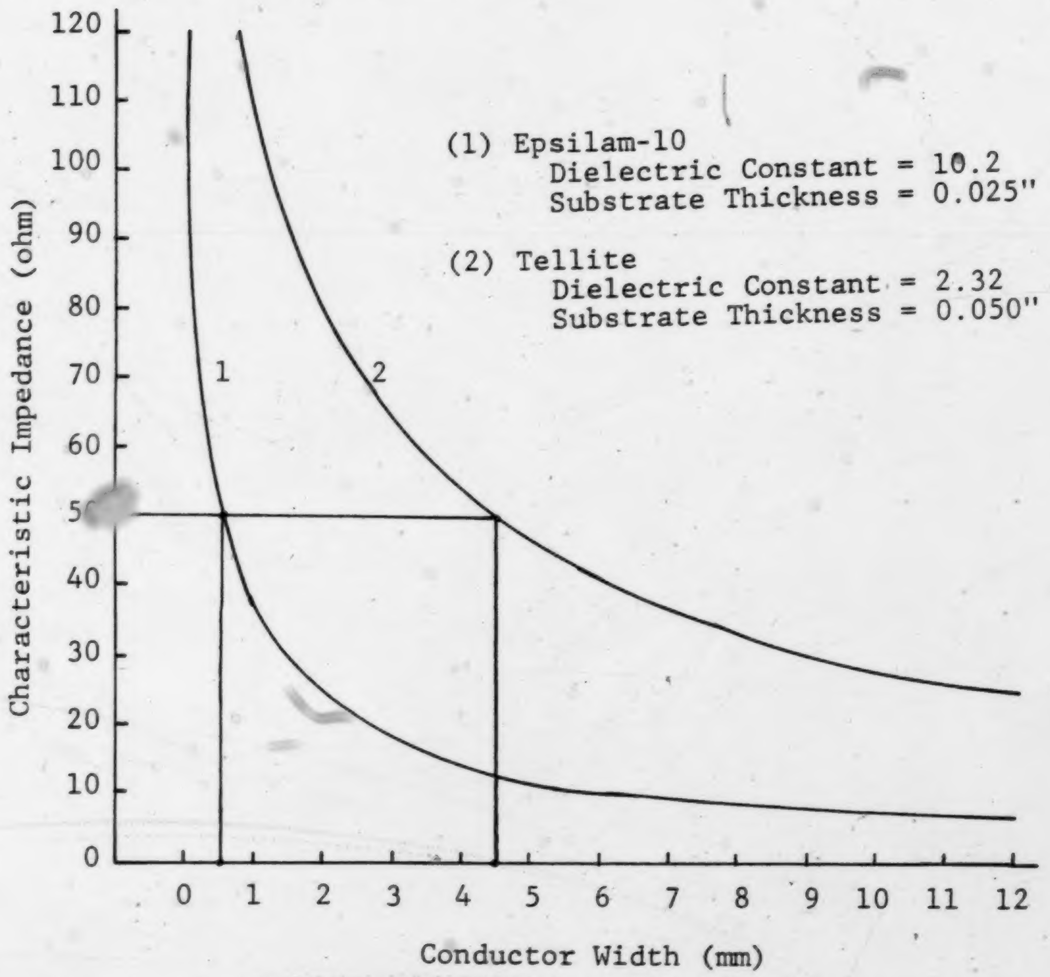


Fig. 2.5 Characteristic Impedance of a Microstrip Line as a Function of Conductor Width

lines are prematurely terminated at the metallic surfaces. These metallic walls can be brought within a spacing of five times the strip width without significantly influencing the microstrip characteristics [2], [24], [25]. These considerations are important in the design of the transistor fixture.

2.6 Microstrip Losses

The information about microstrip losses is important for the characterisation and modeling of the GaAs FET amplifier. Two sources contribute mainly towards microstrip circuit losses, the conductor losses and the substrate dielectric losses. Conductor losses are normally larger than the dielectric losses. For a fixed characteristic impedance, the conductor losses are larger for a thinner substrate and increase with the square root of frequency. The following expressions for microstrip losses have been suggested in the literature [25]

For $1/2\pi < W/h \leq 2$, the conductor loss coefficient

$$\alpha_c = \frac{4.34\sqrt{\pi f\, \mu_o/\sigma}}{\pi Z_o h}\left[1 - \left(\frac{W_e}{4h}\right)^2\right]\left[1 + \frac{h}{W_e} + \frac{h}{W_e \pi}\left(\ln\frac{2\pi}{t} - t/h\right)\right] \tag{2.31}$$

and the dielectric loss coefficient

$$\alpha_d = 4.34\,\frac{\varepsilon_{eff} - 1}{\varepsilon_{eff}\,(\varepsilon_r - 1)}\left(\frac{\mu_o}{\varepsilon_o}\right)^{\frac{1}{2}}\sigma \quad \mathrm{dB}/_{\mathrm{cm}} \tag{2.32}$$

For practical substrate materials used for realising microstrip circuits the losses around 6 GHz typically amount to less than 0.1 dB/cm.

The information regarding microstrip characteristic impedance and losses is used in the amplifier characterisation and modeling process, in the next chapter.

CHAPTER III

COMPUTER-AIDED CHARACTERISATION AND MODELING OF GaAs FETs

In this chapter, a characterisation method is developed for the accurate modeling of the GaAs FET device and the associated microwave circuit. Network analyzer measurements of device scattering parameters have been used with computer-aided design(CAD) programs to realise in-situ device characterisation. The difficulties associated with S-parameters measurements are discussed. Errors in the network analyzer measurements due to imperfections of the system are discussed and a method is described for their removal. Experimental results obtained for a GaAs FET are shown, and the significant features of the device S-parameters and their behavior are discussed.

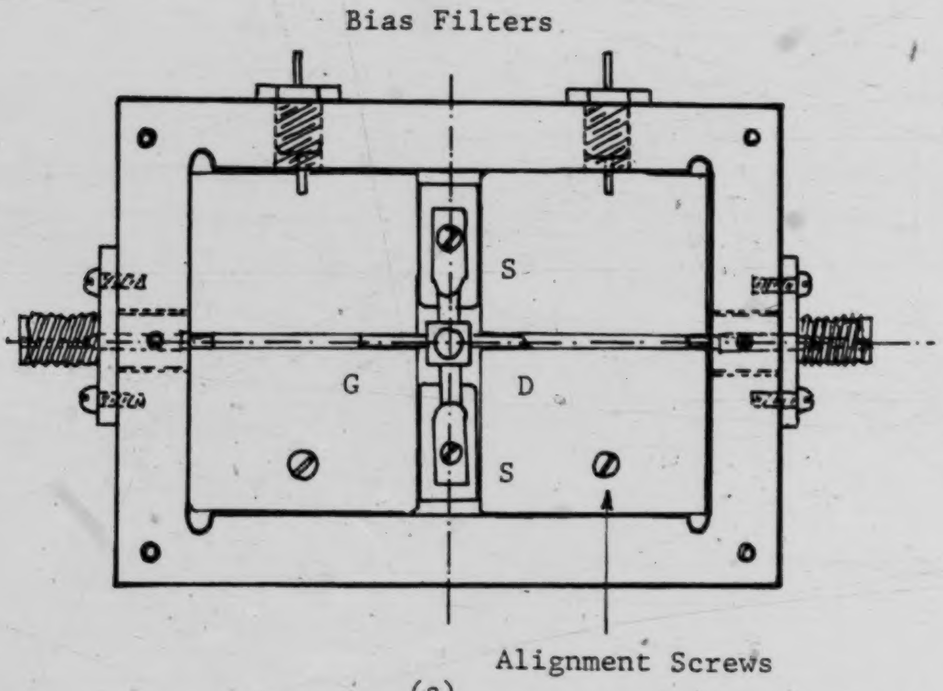
Important aspects of modeling of a GaAs FET device, with particular emphasis on computer reduction of the model from measured S-parameters, are discussed. The use of the CAD approach in the estimation and optimisation of the modeled device parameters is described.

3.1 Introduction

The accurate characterisation of microwave devices is essential for realising amplifiers that meet the design objective. Furthermore, the accuracy of the mathematical model for analysis of the amplifier is dependent on the accuracy of characterisation. Scattering parameter measurements [26]-[28] are normally used for characterisation of devices at microwave frequencies. In order to make the device ports compatible to the measurement system, the device is mounted in a fixture. The mounting of the device causes a transformation of the device parameters through an intermediate network of transmission lines and connectors. Therefore, the device parameters must be de-embedded from the measurements made at the external ports of the fixture. The considerations for the fixture design, the measurement procedure and the de-embedding of the device parameters are described in the following sections.

3.2 Fixture Design:

The size of the fixture depends on the dielectric constant of the microstrip substrate used for making the microwave circuit. Low dielectric constant materials with larger substrate thickness require larger fixtures. Therefore, the high dielectric constant substrate material Epsilam-10 with substrate thickness 0.025 inch was chosen. A fixture of internal dimensions of 1"X1.5" was designed. Figure 3.1 shows the top plan view, and a cross-section from the side-view. One of the significant features of the assembly is that it allows easy replacement of the microstrip circuit, the device, and connectors. One of the main discontinuities can arise at the coaxial-to-microstrip


Bias Filters
S
G
D
S
Alignment Screws
(a)

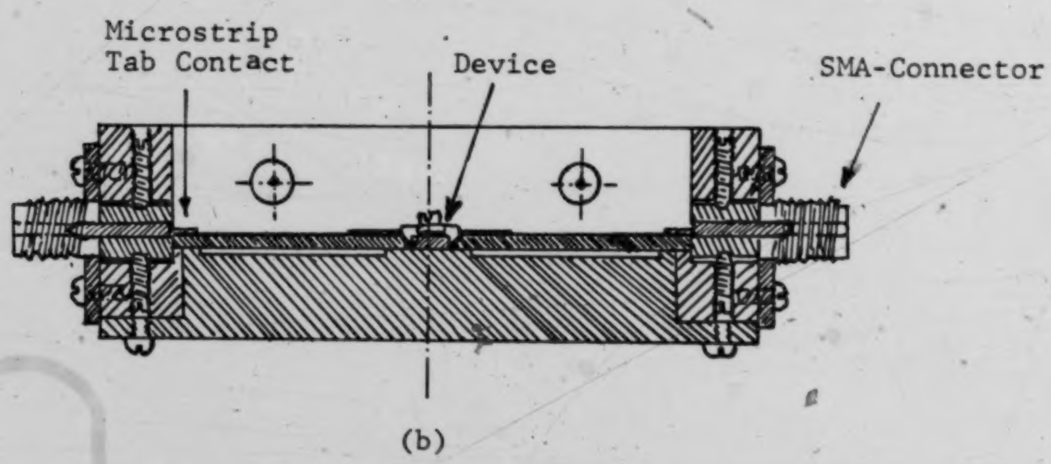

Microstrip
Tab Contact
Device
SMA-Connector
(b)

Fig. 3.1 Fixture Assembly for Mounting the Device

(a) Top View

(b) Cross-section of the Front View

transitions because of an inadvertent open circuit or misalignment. Two screws are provided in the side-walls at the top and bottom of the fixture to ensure a tight and uniform microstrip tab contact. The central alignment is obtained by adjusting the holding screws in the microstrip. The device is held in position by clamping the source leads at the metallic contacts in the bottom plate of the fixture. These metallic contacts are brought to a distance from the microstrip line, approximately five times the width of the line. The microstrip fields are very weak at this distance and do not influence the circuit characteristics. Tight clamping of the source leads ensures a low ground resistance and inductance. A high value of source feedback inductance decreases stability and the maximum stable gain (MSG) of the amplifier [29]. The width of the fixture is 1-inch, which provides enough space for realising the matching and biasing circuits in the microstrip. The width should not be made too large, otherwise waveguide mode fields may be set up within the fixture. The bias filters are provided to filter out any high frequency coupling through the biasing circuit. To make the fixture compatible with the measurement system, adapters are provided to APC-7 connectors but are not shown in Figure 3.1.

3.3 Device mounting

The device is mounted on the microstrip by using teflon posts held in position by metallic screws. The height of the teflon posts is made large enough so that the metallic screws do not influence the field distribution of the microstrip. Such a mounting scheme allows easy removal or replacement of the device during the characterisation process or in case of device burn-out. To realise accurate designs, the reactances introduced by device mounting structure should be included in the characterisation process.

3.4 Measurement set-up

The network analyzer test set-up used for measurement of small-signal S-parameters is shown in Figure 3.2. The set-up uses the HP 8746-B reflection transmission unit with HP 11605A flexible arm for measurements. Biasing to the device is applied through a bias-tee (HP 11590A) on one side and from a biasing element internal to the network analyzer, on the other side. Different parameters are selected by depressing appropriate switches on the front panel of the network analyzer. The power at the RF input of the S-parameter test set must lie in the range from -7 dBm to +9 dBm for the network analyzer to operate properly. The maximum power incident on the test device is of the order of -14 dBm; therefore only small-signal measurements are possible.

The system is calibrated for errors, as described in section 3.5, before starting S-parameter measurements each time. For reflection measurements, initial magnitude and

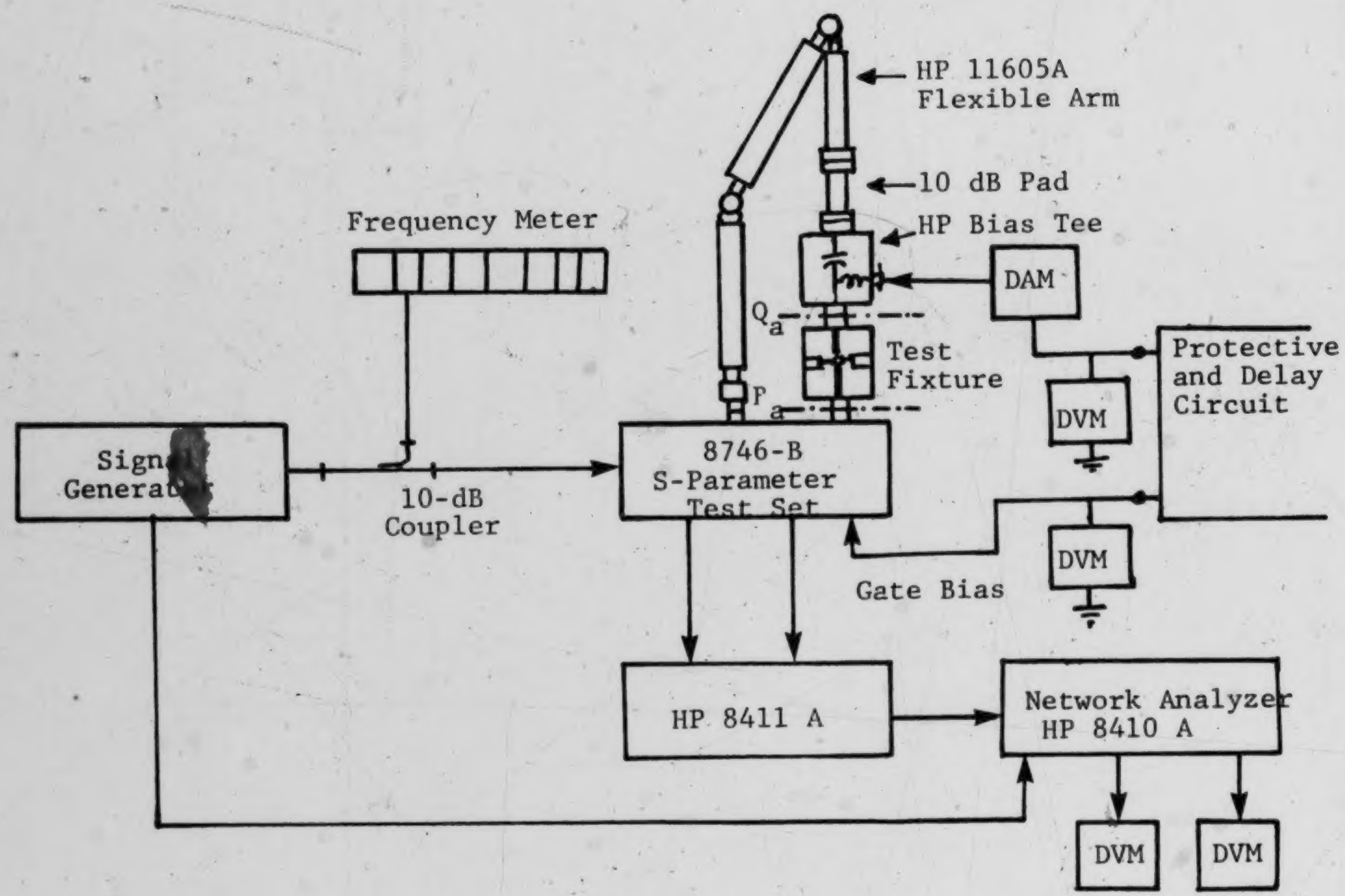

HP 11605A
Flexible Arm
10 dB Pad
HP Bias Tee
Frequency Meter
DAM
Q_a
Test
Fixture
P_a
Protective
and Delay
Circuit
DVM
Sign[illegible]
Generat[illegible]
10-dB
Coupler
8746-B
S-Parameter
Test Set
DVM
Gate Bias
HP 8411 A
Network Analyzer
HP 8410 A
DVM
DVM

Fig. 3.2 Schematic Diagram of the S-parameter Measurement Set-up

phase adjustments are made by putting a short on the network analyzer port. The reflection measurements are made on the fixture with the device, by terminating the other port of the fixture with matched termination. For transmission measurements, a 10-dB pad (HP 8492A) is used with the flexible arm 11605A to attenuate relatively large reflections caused by the flexible arm. Initial phase and magnitude adjustments are made by connecting the flexible arm directly onto the port. Test channel gain is adjusted to compensate for the flexible arm losses and 10-dB pad attenuation and the reference line is extended in the reference channel to adjust for the extra phase due to the lengths of 10-dB pad and the bias-tee . The forward and reverse transmission measurements are made by making transmission measurements in the forward direction only, and by physically reversing the fixture in the test-set.

The frequency of the signal generator is monitored through a 10-dB directional coupler using a digital frequency meter. The measurements were made at a discrete set of frequencies over a frequency range 4.6 GHz to 6.8 GHz, the range over which the network analyzer errors were observed to be a minimum. Two voltages were displayed on the digital voltmeters connected to the display section of the network analyzer; one reading is proportional to the magnitude of scattering parameters (50 mV/dB) and the other is proportional to their arguments (10 mV/degree). The S-parameter measurements were made by applying different bias conditions to the device. The measurements were corrected for errors through an error correction routine, as described in the next section.

3.5 Error-Correction in Network Analyzer

Errors in network analyzer measurements arise mainly because of directivity of the couplers, imperfections in their coupling ratios and reflections from test cables and adapters. All these error terms, which are vector sums of leakage and reflected signals, vary radically as a function of frequency. The necessity of error correction with the S-parameter test set in our laboratory was more pronounced because of large errors observed in measurement. The deviation in the reflected signal with a short on the port was within ±1 dB. Furthermore, the ports of the network analyzer had an offset difference of 1 to 2 dB, making the S-parameter measurements with automatic switching erroneous.

Kruppa and Sodomosky [30] have proposed an explicit solution for removal of network analyzer errors. The method described in this thesis is essentially a modification of their solutions. More complete error correction procedures are discussed in the literature [31],[32]. The problem of error correction in network analyzer is shown in Figure 3.3. It is assumed that an error matrix is interposed between the available ports for measurements and the ports where the device data are recorded. The single error matrix assumption is only a first-order error-correction approximation because

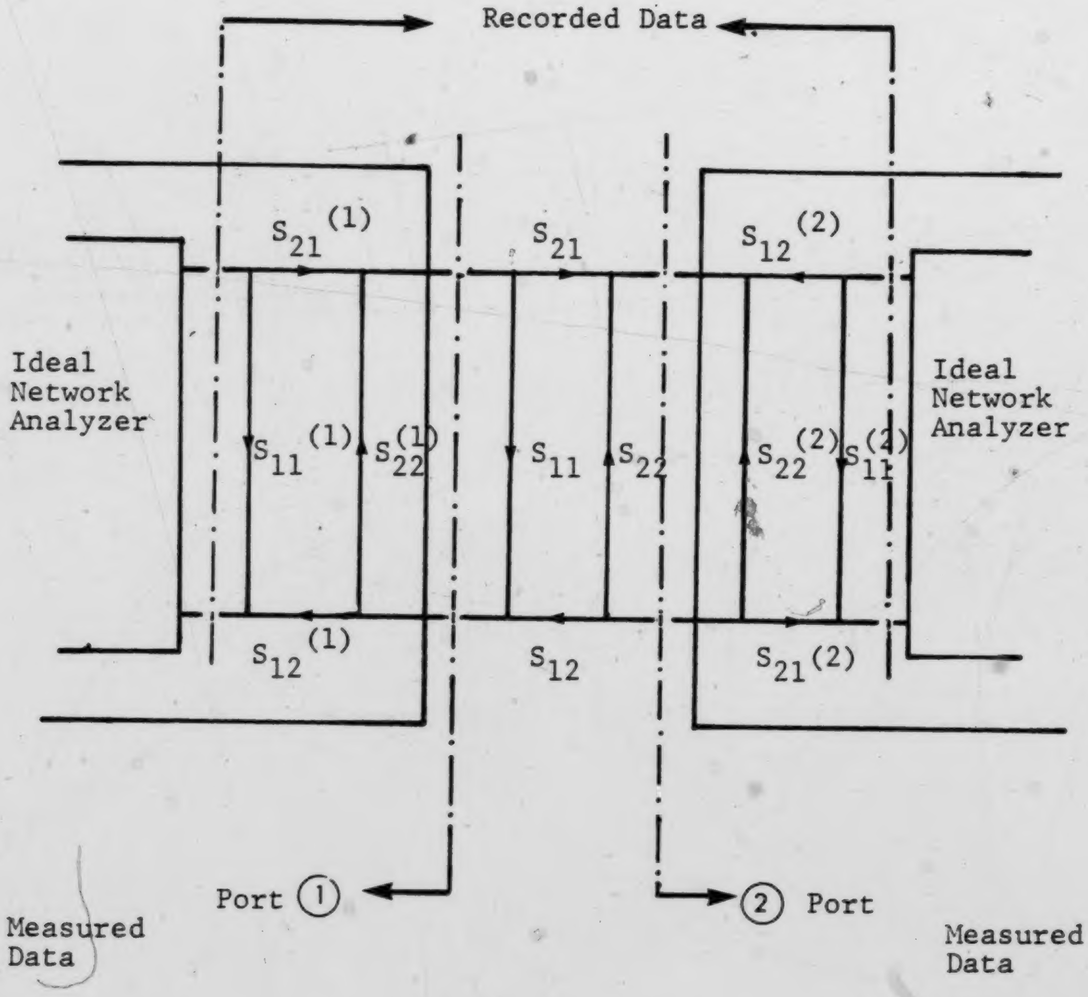

Recorded Data
$S_{21}^{(1)}$
S_{21}
$S_{12}^{(2)}$
Ideal Network Analyzer
$S_{11}^{(1)}$
$S_{22}^{(1)}$
S_{11}
S_{22}
$S_{22}^{(2)}$
$S_{11}^{(2)}$
Ideal Network Analyzer
$S_{12}^{(1)}$
S_{12}
$S_{21}(2)$
Port ①
② Port
Measured Data
Measured Data

Fig. 3.3 Modeling of Errors in the Network Analyzer Measurements

the errors consist of composite errors distributed along the measurement system.

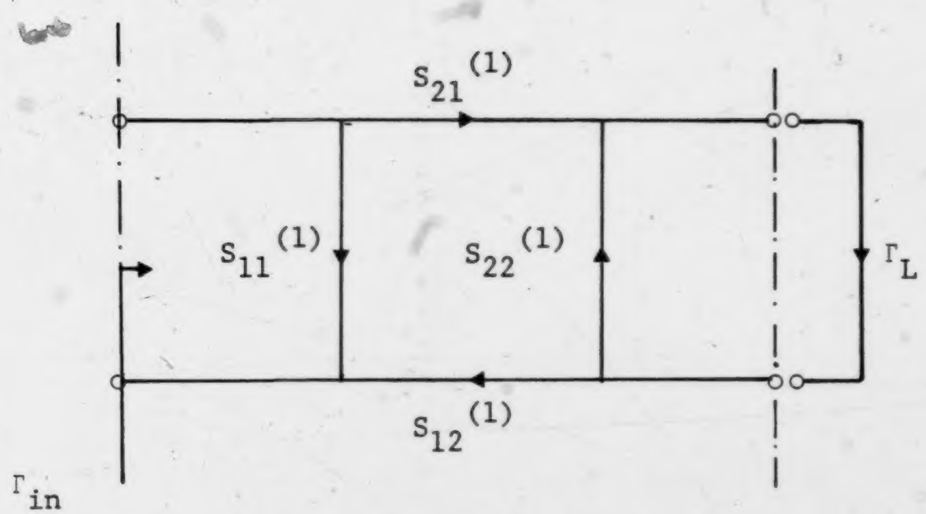
The calibration of errors requires terminating the measurement ports with known loads. At least eight calibration measurements are required; two for transmission coefficients and three for reflection coefficients at each port respectively. A movable short can be used as the known load. The measurements done by the author indicate that a further error source is introduced by this method because the electrical length of the movable short cannot be accurately determined. Matched termination, short circuit, and open circuits were used as calibration standards. Standard match and short circuit terminations are readily available. The open circuit was realised by leaving the APC-7 connectors of the network analyzer open. An equivalent end capacitance [33] of the order of 0.081 pF was included as the effective load. The equivalent electrical load corresponding to physical open circuit at the connectors was computed from

$$\Gamma_L = \frac{\overline{Z}(\omega) - 1}{\overline{Z}(\omega) + 1} \qquad (3.1)$$

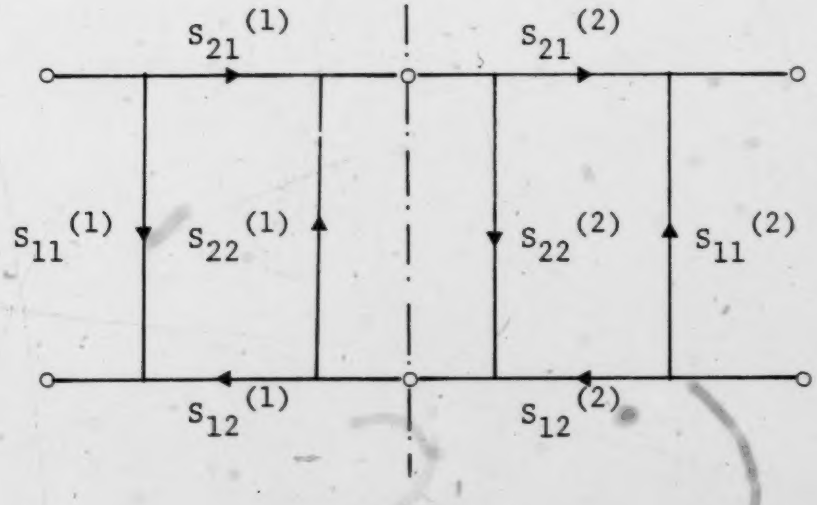
where

$$\overline{Z}(\omega) = -j/\omega.C.Z_o$$

The calibration procedure used for error correction is shown in Figs. 3.4(a) and 3.4(b). The S-parameter variables with superscripts denote the error parameters, and the superscripts 1 and 2 refer to the port of measurement. For a


$S_{21}^{(1)}$
$S_{11}^{(1)}$
$S_{22}^{(1)}$
Γ_L
$S_{12}^{(1)}$
Γ_{in}

(a)


$S_{21}^{(1)}$
$S_{21}^{(2)}$
$S_{11}^{(1)}$
$S_{22}^{(1)}$
$S_{22}^{(2)}$
$S_{11}^{(2)}$
$S_{12}^{(1)}$
$S_{12}^{(2)}$

(b)

Fig. 3.4 Calibration of Errors in the Network Analyzer Measurements

(a) Reflection Coefficient Errors

(b) Transmission Coefficient Errors

known termination at port 1 in Fig. 3.4(a), the input reflection coefficient is given by

$$\Gamma_{in} = S_{11}^{(1)} + \frac{S_{12}^{(1)}\ S_{21}^{(1)}\ \Gamma_L}{1 - S_{22}^{(1)}\ \Gamma_L} \qquad (3.2)$$

For matched, short and open terminations on port 1 the reflection coefficient is given by the following relationships

$$\Gamma_{Fm} = S_{11}^{(1)} \qquad (3.3)$$

$$\Gamma_{Fs} = S_{11}^{(1)} - \frac{S_{21}^{(1)}\ S_{12}^{(1)}}{1 + S_{22}^{(1)}} \qquad (3.4)$$

$$\Gamma_{Fo} = S_{11}^{(1)} + \frac{S_{21}^{(1)}\ S_{12}^{(1)}\ \Gamma_L}{1 - S_{22}^{(1)}\ \Gamma_L} \qquad (3.5)$$

where the subscript F refers to the measurements in the forward direction. From (3.3) and (3.4), one obtains

$$S_{21}^{(1)}\ S_{12}^{(1)} = -(\Gamma_{Fs} - \Gamma_{Fm})\ (1 + S_{22}^{(1)}) \qquad (3.6)$$

and from (3.5)

$$S_{21}^{(1)}\ S_{12}^{(1)} = \frac{(\Gamma_{Fo} - \Gamma_{Fm})\ (1 - S_{22}^{(1)})\ \Gamma_L}{\Gamma_L} \qquad (3.7)$$

from (3.6) and (3.7), $S_{22}^{(1)}$ can be obtained in the following form

$$S_{22}^{(1)} = \frac{\Gamma_{Fo} + \Gamma_{Fs}\ \Gamma_L - \Gamma_{Fm}\ (1 + \Gamma_L)}{(\Gamma_{Fo} - \Gamma_{Fs})\ \Gamma_L} \qquad (3.8)$$

By back substituting (3.3), (3.8) in (3.6), one obtains

$$S_{21}^{(1)}\, S_{12}^{(1)} = -(\Gamma_{Fs} - \Gamma_{Fm})\,(1 + S_{22}^{(1)}) \qquad (3.9)$$

$$= -(\Gamma_{Fs} - \Gamma_{Fm}) \left[1 + \frac{\Gamma_{Fo} + \Gamma_{Fs}\,\Gamma_L - \Gamma_{Fm}\,(1 + \Gamma_L)}{(\Gamma_{Fo} - \Gamma_{Fs})\,\Gamma_L} \right] \qquad (3.10)$$

$$S_{21}^{(1)}\, S_{12}^{(1)} = -\left(\frac{\Gamma_{Fs} - \Gamma_{Fm}}{\Gamma_{Fs} - \Gamma_{Fo}}\right)\left[(\Gamma_{Fo} - \Gamma_{Fm})\left(\frac{1 + \Gamma_L}{\Gamma_L}\right)\right] \qquad (3.11)$$

Similar equations are obtained at port 2. These equations can be obtained from (3.2)-(3.11) by changing the subscript F to R and changing the superscript 1 to 2. Subscript R refers to the reverse direction.

The transmitted signal is obtained by connecting the measurement ports directly using a flexible arm as shown in Fig. 3.4 (b). Test channel gain is adjusted to compensate for the flexible arm losses and 10-dB pad attenuation. The reference line in the network analyzer is extended to compensate for the extra phase shift. The following error transmission coefficients are obtained in forward and reverse direction

$$T_{F_1} = \frac{S_{21}^{(1)}\, S_{12}^{(2)}}{1 - S_{22}^{(1)}\, S_{22}^{(2)}} \qquad (3.12)$$

$$T_{R_1} = \frac{S_{12}^{(1)}\, S_{21}^{(2)}}{1 - S_{22}^{(1)}\, S_{22}^{(2)}} \qquad (3.13)$$

By substituting for $S_{22}^{(1)}$ and $S_{22}^{(2)}$ in equations (3.12) and (3.13), the following relationships can be obtained

$$S_{21}^{(1)}\, S_{12}^{(2)} = T_{F_1}\left[1 - \left[\frac{\Gamma_{Fo} + \Gamma_{Fs}\,\Gamma_L - \Gamma_{Fm}\,(1 + \Gamma_L)}{(\Gamma_{Fo} - \Gamma_{Fs})}\right]\left[\frac{\Gamma_{Ro} + \Gamma_{Rs}\,\Gamma_L - \Gamma_{Rm}\,(1 + \Gamma_L)}{(\Gamma_{Ro} - \Gamma_{Rs})}\right]\right] \tag{3.14}$$

and

$$S_{12}^{(1)}\, S_{21}^{(2)} = T_{R_1}\left[1 - \left[\frac{\Gamma_{Fo} + \Gamma_{Fs}\,\Gamma_L - \Gamma_{Fm}\,(1 + \Gamma_L)}{(\Gamma_{Fo} - \Gamma_{Fs})}\right]\left[\frac{\Gamma_{Ro} + \Gamma_{Rs}\,\Gamma_L - \Gamma_{Rm}\,(1 + \Gamma_L)}{(\Gamma_{Ro} - \Gamma_{Rs})}\right]\right] \tag{3.15}$$

The scattering parameters of the unknown two-ports can be derived using the closed form relations derived by Kruppa and Sodomosky [30]

$$\begin{aligned} S_{11} = (1/D) \Big[(S_{11}^{(M)} - S_{11}^{(1)}) \Big[S_{22}^{(2)} \cdot (S_{22}^{(M)}\, S_{11}^{(2)}) \\ + S_{21}^{(2)}\, S_{12}^{(2)} \Big] - S_{22}^{(2)}\, S_{21}^{(M)}\, S_{12}^{(M)} \Big] \end{aligned} \tag{3.16}$$

$$S_{12} = (1/D)\left[S_{12}^{(M)} \cdot S_{21}^{(1)} \cdot S_{12}^{(2)}\right] \tag{3.17}$$

$$S_{21} = (1/D)\left[S_{21}^{(M)} \cdot S_{12}^{(1)} \cdot S_{21}^{(2)}\right] \tag{3.18}$$

$$\begin{aligned} S_{22} = (1/D) \Big[(S_{22}^{(M)} - S_{11}^{(2)}) \Big[S_{22}^{(1)} \cdot (S_{11}^{(M)}\, S_{11}^{(1)}) \\ + S_{12}^{(1)}\, S_{21}^{(1)} \Big] - S_{22}^{(1)} \cdot S_{21}^{(M)} \cdot S_{12}^{(M)} \Big] \end{aligned} \tag{3.19}$$

where

$$\begin{aligned} D = \Big[\Big[S_{21}^{(1)}\, S_{12}^{(1)} + S_{22}^{(1)}\, (S_{11}^{(M)} - S_{11}^{(1)}) \Big] \\ \Big[S_{21}^{(2)}\, S_{12}^{(2)} + S_{22}^{(2)}\, (S_{22}^{(M)} - S_{11}^{(2)}) \Big] \\ - S_{22}^{(2)} \cdot S_{22}^{(1)} \cdot S_{12}^{(M)} \cdot S_{21}^{(M)} \Big] \end{aligned} \tag{3.20}$$

$S_{11}^{(M)}, S_{22}^{(M)}, S_{21}^{(M)}, S_{12}^{(M)}$ are the measured values of the reflection and transmission coefficients. It may be pointed out here that the error coefficients are a function of the operating frequency. Therefore, an error characterisation run is made at the discrete set of frequencies at which the device S-parameters are to be measured. The S-parameters of the device were measured by physical reversal of the transistor fixture; therefore further simplification of above equations results. The simplification is obtained by substituting $S_{ij}^{(1)}=S_{ij}^{(2)}$. For the fixture characterisation, single-port error correction is essential. The relationships for single-port error characterisation can be derived from Fig. 3.4(a). From equation (3.2) the measured reflection coefficient is given by

$$\Gamma_{in}^{(M)} = S_{11}^{(1)} + \frac{S_{12}^{(1)}\ S_{21}^{(1)}}{1/\Gamma_L - S_{22}^{(1)}} \tag{3.21}$$

From (3.20), solving for unknown reflection coefficient, one obtains

$$\Gamma_L = \cfrac{1}{S_{22}^{(1)} + \cfrac{S_{12}^{(1)}\ S_{21}^{(1)}}{\Gamma_{in}^{(M)} - S_{11}(1)}} \tag{3.22}$$

The error parameters in (3.22) are obtained by making measurements with matched, short and open terminations on each port and using (3.3) to (3.7).

3.6 Device Characterisation and Modeling

The characterisation process involves measurement of the S-parameters at the external fixture ports and then their transformation to the device reference ports. Figure 3.5 depicts a schematic of the overall fixture for de-embedding of the device parameters. P_a and Q_a refer to the external ports of the fixture where the measurements are made and P_d and Q_d to the device ports to which the transformation must be made. The intermediate network consists of the 50-ohm microstrip line, the coaxial-to-microstrip transitions and the connectors at both the ports.

A method for de-embedding of parameters has been described by Ajose et al. [34],[35]. The method involves measurement of the input impedance at the connector ports by using open-circuited microstrip lines of different lengths. A transmission matrix for the intermediate networks at both ports is computed and the device parameters are obtained by matrix inversion. This method requires changing the microstrip circuit a number of times and is excessively cumbersome.

Another method for de-embedding the device parameters has been described by Cooper and Gupta [36],[37] using the microwave analysis computer program 'MARTHA'. The method uses a nodal shift experiment which involves measurement of input reflection coefficients with different loads at the output. Such a characterisation procedure requires known

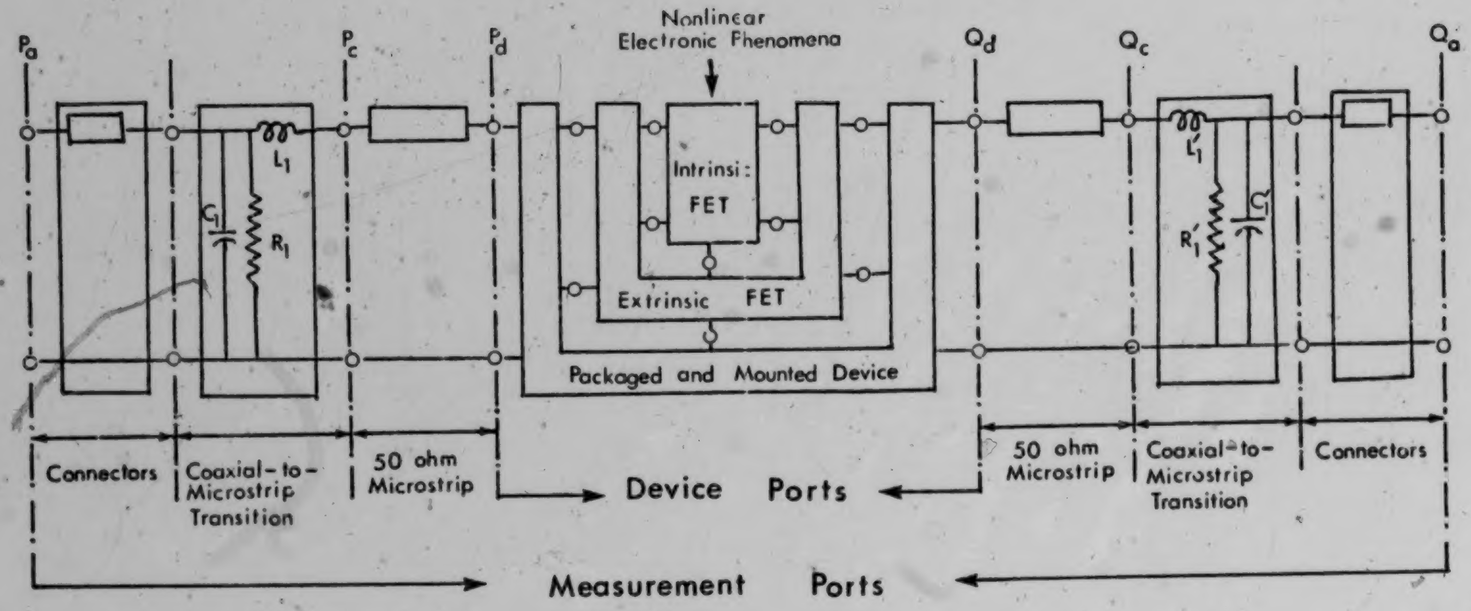

P_a
P_c
P_d
Nonlinear Electronic Phenomena
Q_d
Q_c
Q_a
L_1
C_1
R_1
Intrinsi: FET
Extrinsic FET
Packaged and Mounted Device
L_1'
R_1'
C_1'
Connectors
Coaxial-to-Microstrip Transition
50 ohm Microstrip
Device Ports
50 ohm Microstrip
Coaxial-to-Microstrip Transition
Connectors
Measurement Ports

Fig. 3.5 Schematic Diagram of the Overall Fixture for De-embedding of the Device Parameters

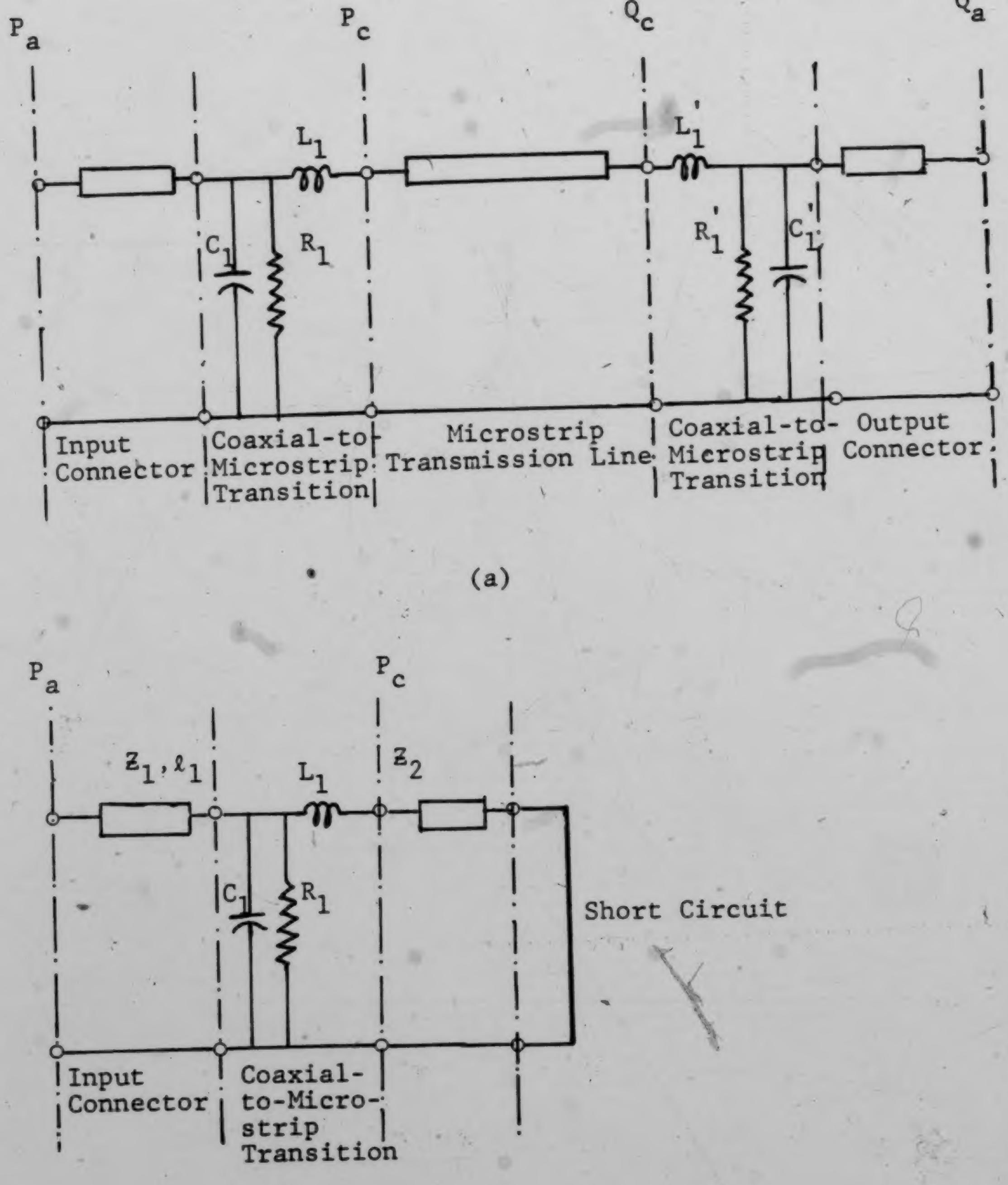
calibration standards that could be accommodated in the space reserved for mounting the device. Whereas it is relatively easy to realise a microwave short circuit, it is very difficult to realise an circuit and a matched termination that can be mounted in place of the device.

A method of device characterisation is proposed in HP Application note 117-2 [38]. An HP 11608A standard fixture is used for transistor characterisation. In this method, the fixture is represented as lengths of transmission line up to the planes of the device mounting. This length is compensated by introducing equivalent line lengths in the reference channel of the network analyzer. The method has the advantage of being fast, but the accuracy of the measurement is degraded because of excess reactances associated with the fixture and the device mounting. The effect of these reactances on the device parameters is further discussed in section 3.7. Furthermore, the errors associated with the network analyzer as discussed in section 3.5 cannot be conveniently corrected.

Because of the difficulties of characterisation described above, none of these methods was found suitable for accurate device characterisation. A method was therefore developed that combines and refines the significant concepts of the above techniques. It features a) the use of a network analyzer for rapid measurements, b) the use of CAD programs for modeling of the fixture and the device, c) the measurement of the device S-parameters in the same fixture and under same mounting conditions as used in the final amplifier, d) the de-embedding of the device parameters from the circuit and e) computer removal of network analyzer errors.

3.6.1 Fixture Modeling

The fixture was modeled by measuring the two-port S-parameters over a discrete set of frequencies with a 50-ohm line between the connectors. The single-port and two-port error correction discussed in the section 3.5 was applied for these measurements. For the purpose of device characterisation the biasing is applied externally whereas in the final amplifier the biasing is integrated with the amplifier. Therefore, no dc blocking capacitors were used during characterisation. In the final amplifier configuration the dc blocks were used to isolate RF from dc. For modeling of the fixture therefore, the S-parameters were measured both with and without dc blocking capacitors. The input and output connectors were modeled as lengths of transmission lines of impedances Z_1 and Z_1', lengths l_1 and l_1 and loss factors $\alpha_1$and α_1' respectively. Since similar Amphenol APC-7 and ARM 2052-1133 SMA/microstrip connectors were used at both the input and output ports of the fixture these characteristics were modeled to be same at both the ports. The loss factors $\alpha_1$and α_1' have a typical value of 0.1 dB/guide wave-length at 5 GHz and were modeled to increase as the square-root of frequency. The microstrip was modeled as a length of transmission line of impedance Z_2 and length l_2. The loss factor associated with the microstrip line was assumed to be zero, because microstrip losses are relatively small. The modeling of the intermediate coaxial-to-microstrip transitions has been studied by Wight et al. [39]. They obtained a two element equivalent circuit model for a launcher transition. The equivalent circuit was obtained from measurement of excess phase in the input reflection coefficient as the lengths of open-circuited microstrip lines were changed. Each transition introduces an excess phase shift of the order of 20 to 30 degrees. The parallel resistance in the model is introduced to account for losses at the transitions. The network topology for the overall fixture model is shown in Fig. 3.6(a). The final modeled parameters were obtained by least-square fitting the overall fixture model to the measured two-port S-parameters by use of computer program COMPACT [40]. The initial values for the modeled equivalent transmission line lengths were specified as equivalent phase shifts at 5 GHz, computed from the physical line lengths. The initial value of line impedance was chosen to be 50 ohms. The starting equivalent circuit values for coaxial-to-microstrip transitions were obtained from the experimentally observed values reported in [39]. Using the initial values of the circuit elements, the computer program COMPACT computes the S-parameters of the model. The calculated S-parameters of the model are compared with the measured parameters and selected network elements


P_a
P_c
Q_c
Q_a
L_1
L_1'
C_1
R_1
R_1'
C_1'
Input Connector
Coaxial-to-Microstrip Transition
Microstrip Transmission Line
Coaxial-to-Microstrip Transition
Output Connector
P_a
P_c
Z_1, ℓ_1
L_1
Z_2
C_1
R_1
Short Circuit
Input Connector
Coaxial-to-Micro-strip Transition

(a)

(b)

Fig. 3.6 Network Topology for Modeling of the Fixture

(a) Overall Fixture Between External Ports

(b) Verification of the Fixture Model

are varied to minimize a predefined error function. For least-square fitting, the error function is defined in the following form

$$E.F. = \frac{1}{N}\sum_{F=F_1}^{F_N}\left\{W_1\cdot\left|S_{11_M} - S_{11_C}\right|^2 + W_2\cdot\left|S_{22_M} - S_{22_C}\right|^2 + W_3\cdot\left|S_{21_M} - S_{21_C}\right|^2 + W_4\cdot\left|S_{12_M} - S_{12_C}\right|^2\right\} \quad (3.23)$$

where subscripts M and C refer to measured and calculated values of the S-parameters.

A minimum error function of value 0.421 was obtained for weighing factors W_1, W_2, W_3 and W_4 of 10 each. The agreement obtained between measured and computed S-parameters was within 0.110 in magnitude and ±10 degrees in phase. The final optimised values are listed in Table 3.1. The characteristic impedance of the equivalent transmission line for the connectors is observed to be 50.9 ohms without dc blocking capacitors and 51.52 ohms with dc blocking capacitors, indicating the extra discontinuity introduced by using dc blocking capacitors. The impedance of the microstrip is modeled to be 48.4 ohms instead of 50 ohms, the discrepancy being due to fabrication and etching tolerances. To varify the accuracy of the modeled fixture parameters, a microwave short-circuit was placed in the space designed for mounting the device and the input reflection coefficient was measured. The short circuit was

Table 1 Modeled Parameter Values for the Distributed Circuit

Input and Output Coaxial Connectors		Input Circuit		† Output Circuit	
Without D.C. Blocking Capacitor	With D.C. Blocking Capacitor	Coaxial-to-Microstrip Transition	Matching Circuit	Coaxial-to-Microstrip Transition	Matching Circuit
$Z_1 = Z'_1 =$ 50.9 ohm $^*\alpha_1 = \alpha'_1 =$ 0.1 dB/λ_g at 5 GHz $\ell_1 = \ell'_1 =$ 314° at 5GHz	$Z_1 = Z'_1 =$ 51.52 ohm $\alpha_1 = \alpha'_1 =$ 0.1 dB/λ_g at 5 GHz $\ell_1 = \ell'_1 =$ 427.3 at 5GHz	$L_1 =$ 0.095 nH $C_1 =$ 0.187 pF $R_1 =$ 962 ohm	$Z_2 =$ 48.4 ohm $\alpha_2 = 0$ (assumed) $\ell_2 = 662$ mil $\ell_3 = 31$ mil $\ell_4 = 112$ mil	$L'_1 =$ 0.149 nH $C'_1 =$ 0.154 pF $R'_1 =$ 947.0 ohm	$Z'_2 =$ 48.4 ohm $\alpha'_2 = 0$ (assumed) $\ell'_2 = 640$ mil $\ell'_3 = 42$ mil $\ell'_4 = 236$ mil

* Loss factors α_1 and α_1' increase as square root of frequency

† Primed parameters refer to the output circuit. The output circuit has the same topology as the input circuit.

realised by machining a copper piece to fit the space designed for mounting of the transistor. A copper conductor line of width equal to the metal conductor on the microstrip line was bonded on the metal piece by using a conductive epoxy. The measured reflection coefficients at both the ports were compared with the computed reflection coefficients. An agreement was obtained within 0.103 in magnitude and ±10 degrees in phase indicating the validity and accuracy of the fixture model.

3.6.2 Device Modeling

The choice of a particular device model is normally a compromise between its complexity and accuracy. Simple device models tend to be reasonably accurate over a limited frequency range and a fixed set of bias conditions. However, more generalised models that are accurate over larger bandwidths and different biasing conditions must include a complete representation for the active device and a representation for the package parasitics.

Borrego et al. [41] have derived equivalent circuit parameters of a model from measurements at 1 MHz. Such a modeling technique has the convenience of being simple, but the accuracy of the method is very limited. The value of the package parasitics, channel resistance, and gate metallisation resistance cannot be measured by this method.

Simplification in models has been proposed [42] by ignoring the feedback source resistance and inductance. The effect of these feedback elements on the maximum stable gain and stability has been studied [29], [43]. For accurate modeling of a device these elements should be included in the models.

An effective and accurate method of modeling a device is by fitting the calculated S-parameters of the model to the measured device S-parameters, by use of computer optimisation and analysis programs [44]. A circuit topology, shown in Figure 3.7, was selected for device representation. The origin of various circuit elements has been discussed in section 2.4 and 2.5 and is shown in Figure 2.3. The device model is same as described by Ohkawa et al. [45], and includes the effect of feedback elements such as the drain-gate Miller capacitance C_{dg}, and source-resistance R_s and inductance L_s. The drain-to-channel feedback capacitance considered in [4] and [43] is, however, ignored because of its small value [32]. The value for intrinsic device elements was obtained from device physics relationships (2.19), (2.20) and (2.21) discussed in section 2.4.1. The initial value of device transconductance g_m, can also be readily obtained from observation of the forward gain parameter S_{21} [44], by using

$$\begin{aligned} S_{21} &= -2g_m\ Z_o \\ &= -100\ .g_m \end{aligned}$$

for Z_o= 50 ohm. (3.24)

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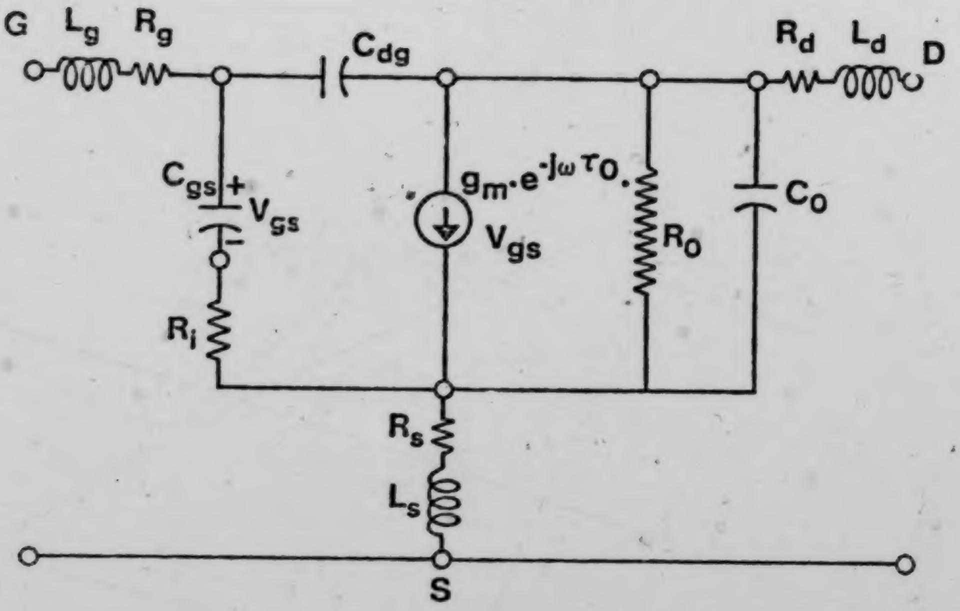
G
L_g
R_g
C_{dg}
R_d
L_d
D
C_{gs}
+
V_{gs}
-
$g_m \cdot e^{-j\omega\tau_o} \cdot$
V_{gs}
R_o
C_o
R_i
R_s
L_s
S

Device Model

Fig. 3.7 Lumped Circuit Model for the GaAs FET. The Model Includes the Effect of Feedback Elements

Table II

Modeled device parameter values for $V_{DS} = 3.0V$, $V_{GS} = -1.0$ V

Parameter	Value	Parameter	Value
L_g	1.28 nH	g_m	34.18 mmho
R_g	1.837 ohm	τ_o	12.9 psec
C_{gs}	0.529 pF	R_o	465.9 ohm
R_i	1,15 ohm	C_o	0.4364 pF
R_s	1.1 ohm	R_d	4.875 ohm
L_s	0.16 nH	L_d	0.663 nH
C_{dg}	0.0514 pF		

The time delay parameter τ_o, which arises because of finite saturation velocity of electrons along the device channel, can be calculated by using

$$\tau_o = \frac{L}{V_s} \tag{3.25}$$

For 1 µm gate-length device with saturated velocity of 1.67×10^5m/sec, the approximate value of τ_o is 6 psec. The gate and drain package inductance L_g and L_d were taken to be 0.5 nH as typical values and the source inductance value of 0.2 nH was selected. The output capacitance C_o was modeled to be 0.2 pF. The extrinsic resistances R_d, R_g and R_s were estimated from dc measurements on the device near the origin of voltage current slopes [36],[37]. The resistance in the drain circuit was measured by applying a small forward gate current and measuring the voltage across the source-drain terminals. Similarly, the source resistance was measured by changing the drain source interconnection.

$$R_d = \frac{\Delta V_{sd}}{\Delta I_{gd}} \tag{3.26}$$

$$R_s = \frac{\Delta V_{sd}}{\Delta I_{gs}} \tag{3.27}$$

The values of R_d and R_s were estimated to be approximately 5.2 ohm and 2.5 ohm respectively. The gate-resistance R_g was obtained by measuring the drain-to-gate voltage for small forward gate current

$$R_g = \frac{\Delta V_{dg}}{\Delta I_{gs}} \tag{3.28}$$

The value for R_g was thus estimated to be 2.2 ohm.

The parameters of the fixture with the device were measured by using the measurement set-up described in section 3.4 with a network analyzer system. These measured parameters were error-corrected using the equations described in section 3.5. The measurements were made with different drain and gate biasing on the device. Using the modeled fixture parameters and estimated device parameters, the composite S-parameters of the fixture and device were computed. These calculated parameters were least-square fitted to the measured composite S-parameters by using the computer program COMPACT [15]. Following error function was defined

$$E.F. = \frac{1}{N} \sum_{F = F_1}^{F_N} \left\{ W_1 \cdot \left| S_{11_M} - S_{11_C} \right|^2 + W_2 \cdot \left| S_{22_M} - S_{22_C} \right|^2 + W_3 \cdot \left| S_{21_M} - S_{21_C} \right|^2 + W_4 \cdot \left| S_{12_M} - S_{12_C} \right|^2 \right\} \quad (3.29)$$

W_1, W_2, W_3, and W_4 are the weighting functions and their values were selectively chosen to get the best fit with a minimum of computer time.

Advantage was taken of the fact that the reverse isolation parameter S_{12} for GaAs FETs is very small. Therefore the input parameter S_{11} is largely determined by the elements L_g, R_g, C_{gs}, and R_i. Therefore, a first run was made by fitting S_{11} alone with these four parameters as variables making W_2 , W_3 and W_4 zero. Similarly the output reflection parameter S_{22} is largely determined by the elements in the output circuit such as R_o , C_o , R_d and L_d . In the second run W_3 and W_4 were kept zero, and the fitting was done for S_{22} alone making R_o , C_o , R_d and L_d as variables. During the third optimisation step, only W_4 was maintained zero and fitting was done for forward gain parameter S_{21} alone with parameters g_m , C_{gs} and R_o being the variables. With each optimisation step the error function reduced significantly. In the next step all the weighting functions were assigned equal weight and S_{12} was included in the optimisation process by making C_{dg} , R_s and L_s as variables.

Once this initial optimisation process is completed, a final fine tuning run was made by taking all the circuit parameters as variables, and a quick convergence was obtained in this step. It was observed that the reverse parameter S_{12} was most difficult to fit. Further improvement can be obtained in the fit by increasing the weight W_4 [40] and going through another optimisation iteration. The measurement and fitting was done over a frequency range from 4.6 GHz to 6.8 GHz over a discrete set of frequencies. Because of 13 elements in the device model, at least 13 frequencies will be required at which the measurement should be made. A larger number of frequencies should be used for obtaining a better fit of the model. Once the optimisation process is completed, the device scattering parameters can be obtained from the device model. The final optimised values of the equivalent circuit elements of an HP HFET-1101 GaAs FET device are listed in Table 3.2.

The advantage of using this scheme is that the measurements need to be made over a limited range of frequencies and from the device model it is possible to calculate the device scattering parameters at all frequencies of interest. Another advantage is that any random errors associated with the network analyzer measurements are removed during the optimisation process.

3.7 Measurement results

The de-embedded parameters for an HP HFET-1101 GaAs FET are shown in Figs. 3.6 and 3.7. The input and output reflection parameters S_{11} and S_{22} for GaAs FETs remain capacitive over large frequency ranges [4],[40],[41]. Any excess reactances, however, transform these parameters over the Smith Chart. Such reactances may be introduced by mounting scheme of the device in the fixture. It is observed in Figure 3.6, for example that the measured S_{11} for the device is inductive at frequencies above 6 GHz. Another set of parameters was obtained by reducing the gate parasitic reactance from 1.29 nH to 0.29 nH, and S_{11} is observed to be capacitive over the frequencies shown. The path of transformation is shown by the dotted lines. It is evident that parasitics affect S_{11} more significantly towards higher microwave frequencies. This observation also underlines the

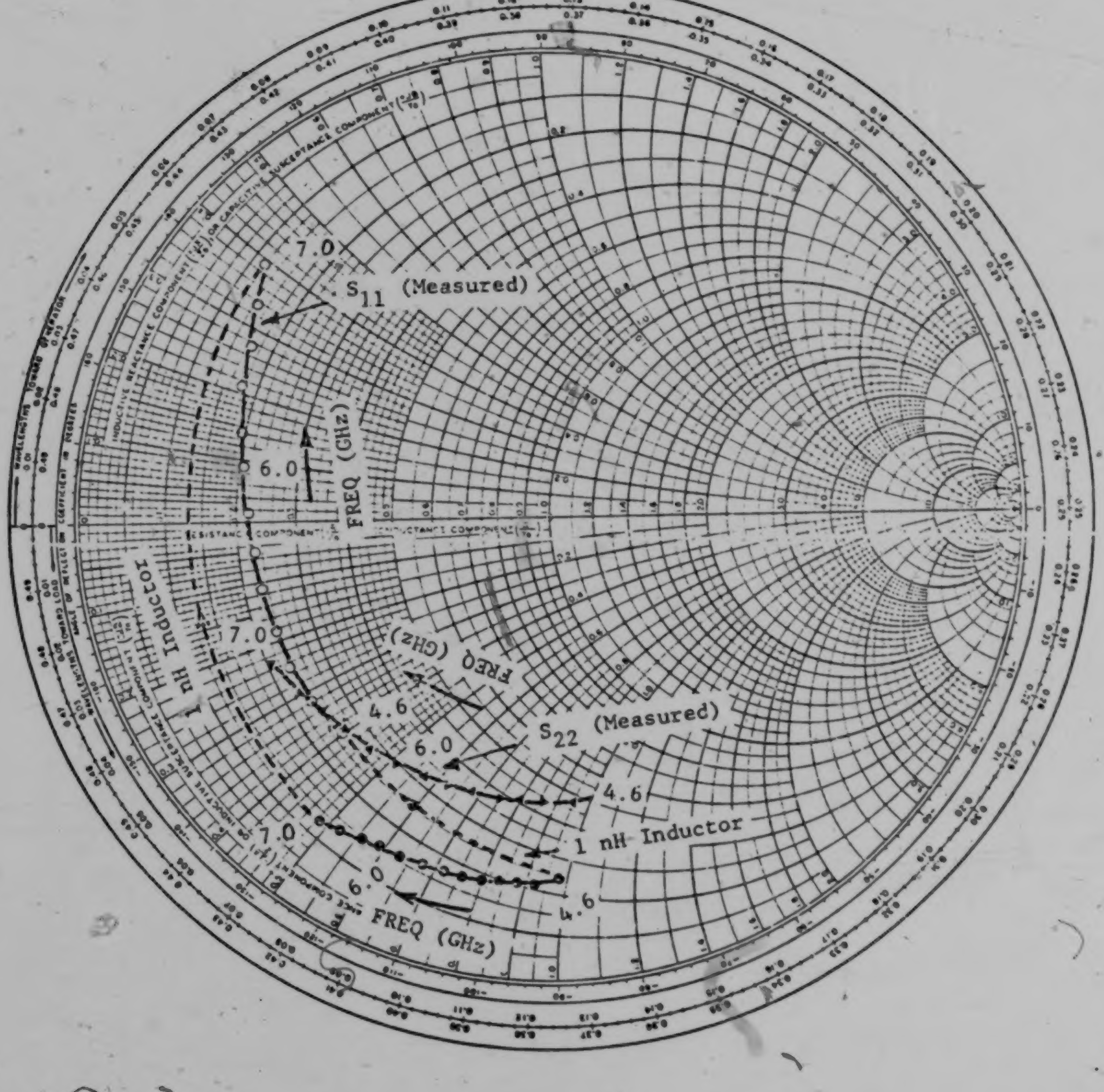

Fig. 3.8 The Measured Input and Output Reflection Parameters S_{11} and S_{22} for an HP HFET-1101 GaAs FET. V_{DS} = 3.0V, V_{GS} = -1.0V

importance of accurate characterisation and modeling of the device. S_{22} is observed to remain capacitive over the measured frequency range.

The results for the forward gain and reverse isolation parameters are shown in Fig. 3.7. The dependence of these parameters on frequency and gate-bias is indicated by arrows. It is observed that S_{21} decreases in magnitude as a function of frequency. This inherent roll-off of S_{21} with frequency should be compensated by a matching network with opposite frequency slope for broad-band amplifier designs. Also S_{21} decreases in magnitude as the gate-bias on the FET is made more negative. The reverse parameter S_{12} is observed to increase with increasing frequency and its dependence on the gate bias is small. As discussed in the next chapter the stability of the amplifier is dependent on the product of S_{21} and S_{12}, therefore the amplifier has a tendency to be unstable at higher microwave frequencies. These measured parameters form the basis for further design and realisation of a GaAs FET amplifier.

In the characterisation procedure described in this chapter, an effort has been made to minimise the errors arising because of imperfections of the connectors and directional couplers in the network analyzer. The errors arising because of inherent drift in the network analyzer and because of temperature changes, however, can not be removed. The magnitude of the reverse isolation parameter S_{12} is comparable to the errors within the measurement

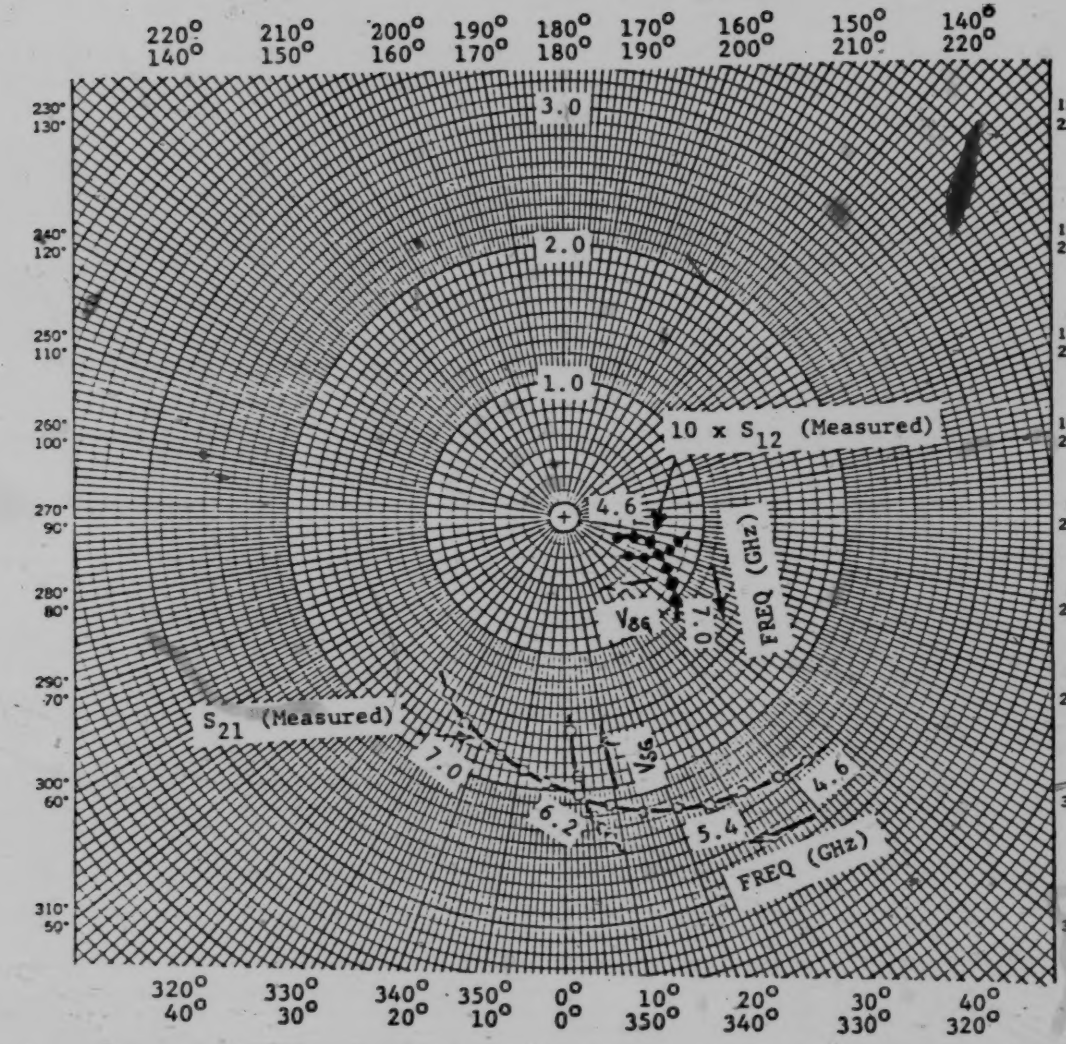

Fig. 3.9 The Measured Forward Gain and Reverse Isolation Parameters S_{21} and S_{12} for HP HFET-1101 GaAs FET; V_{DS} = 3.0V, V_{GS} = 1.0V

system; therefore its accuracy cannot be adequately estimated. The parameters S_{11}, S_{22}, and S_{21} are estimated to be accurate within 10%.

CHAPTER IV

GaAs FET AMPLIFIER DESIGN AND PERFORMANCE

In this chapter, results from an actual GaAs FET amplifier are summarised. Relevant equations are described for the amplifier gain and stability parameters. The considerations for selection of source and load matching circuits and the biasing scheme are outlined. A distributed model of the overall amplifier is described, and computed results for the amplifier small-signal gain and phase response are shown. Comparison is made with experimentally measured results.

4.1 Introduction:

Measured device S-parameters can be used to design the source and load terminations to realise a stable amplifier. Initial approaches for the design of amplifiers have involved cut-and-try methods, where the amplifier is tuned in order to obtain the desired frequency response. Exact synthesis procedures are now available [14], [46],[47], that allow design of the input and output matching networks for realising desired gain bandwidth characteristics. Using these synthesis techniques amplifiers have been realised, with more than an octave bandwidth [2]. The use of computer-aided design programs further allows computation of the amplifier response, and the final circuit can be optimised to obtain the best possible response. For narrow-band amplifier designs, the measured device parameters can be used to design the matching circuits using a Smith Chart [48]. The use of a CAD program such as COMPACT, allows evaluation of the overall amplifier response before the amplifier is actually fabricated. The design relationships have been discussed in a number of papers [48],[49], in terms of device S-parameters. For the sake of completeness, these will be discussed again in the next section.

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4.2 Amplifier Gain and Stability Relationships:

The use of the Smith Chart as a design aid is based on two major considerations: a) the assumption of unilateral gain ($S_{12}=0$) and b) the construction of constant-gain circles on the Smith Chart. The unilateral transducer power gain of a transistor amplifier is given by [48],[49]

$$G_{T_u} = \frac{(1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} \cdot |S_{21}|^2 \cdot \frac{(1 - |\Gamma_L|^2)}{|1 - S_{22}\Gamma_L|^2} \tag{4.1}$$

$$= G_S \cdot G_O \cdot G_L$$

$$= G_S(\mathrm{dB}) + G_O(\mathrm{dB}) + G_L(\mathrm{dB})$$

where S_{11}, S_{22}, and S_{21} are the device S-parameters and the reverse isolation parameter S_{12} has been assumed to be zero. Γ_S, and Γ_L are the reflection coefficients of the source and load matching terminations respectively. G_O is

2

the inherent gain of the device due to forward gain parameter S_{21} . G_S and G_L represent the gain contributions because of matching at the source and load ports respectively. The expressions for G_S and G_L in (4.1) can be solved for a set of source and load reflection coefficients that yield constant gain contributions. These contours are in the form of circles; known as constant gain circles. Maximum gain is obtained by a simultaneous conjugate match at the source and load ports. For an unilateral assumption, therefore, the source and load reflection coefficients for a conjugate match are given by

$$\Gamma_S = S_{11}^* \tag{4.2}$$

$$\Gamma_L = S_{22}^* \tag{4.3}$$

In practical devices, however, the parameter S_{12} is not zero, and the effective input and output S-parameters of the device are a function of the source and load impedances. For simultaneous conjugate match, the required source and load impedances at each frequency of interest can be obtained from the closed form solutions of the following form [48],[49]

$$\Gamma_S = C_S^* \frac{B_S \pm \sqrt{B_S^2 - 4|C_S|^2}}{2|C_S|^2} \tag{4.4}$$

where

$$C_S = S_{11} - \Delta S_{22}^* \tag{4.5}$$

$$B_S = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{4.6}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{4.7}$$

The above relationships are obtained for source impedance. The corresponding relations for the load impedance can be obtained by changing the subscript S to L, and interchanging subscripts 11 and 22. The transducer gain for the amplifier is given by

$$G_T = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S|^2} \qquad (4.8)$$

Equation (4.1) can be obtained from (4.8) by substituting $S_{12} = 0$.

Before realising the actual amplifiers, the stability of the amplifier must be checked. A stability factor K may be defined in terms of the device scattering parameters as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \qquad (4.9)$$

where

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \qquad (4.10)$$

K greater than unity ensures that the amplifier is unconditionally stable. For K less than unity, the regions of instability can be computed from the device S-parameters by using the expressions described in [48] and [49]. The source and load termination should lie only in the stable region of the Smith Chart. Since the device S-parameters are dependent on the signal frequency and device biasing, the stability should be checked at all frequencies and operating biases.

4.3 Design and Realisation of GaAs FET Amplifier:

The basic amplifier configuration is shown in Fig.4.1. A protective and delay circuit is used in the bias supply to first apply negative gate-bias before applying the drain potential during switch-on. Furthermore, it protects the device from any bias-supply transients. A complete schematic of the protective and delay circuit is given in Appendix-I. A variable resistance in the drain circuit is used to vary the drain potential. The bias filters are provided for high frequency decoupling of the device from the biasing circuit. The dc blocking capacitors are used at the input and output circuits to isolate the RF source from the dc supply. The matching circuits can be conveniently designed by using the measured device S-parameters and a Smith Chart. Since the objective of the design is to realise a relatively narrow band amplifier, open circuit single stubs are used both at the input and output circuits of the amplifier. Larger bandwidths could be realised by placing stubs as close to the device as possible. The stability circles [48], [49] were computed from the measured device S-parameters, at various frequencies of interest. From these circles, the unstable regions were defined on the Smith Chart as shown in Fig. 4.2. The conjugate source and load terminations, for an unilateral device assumption, are also shown on the Figure.

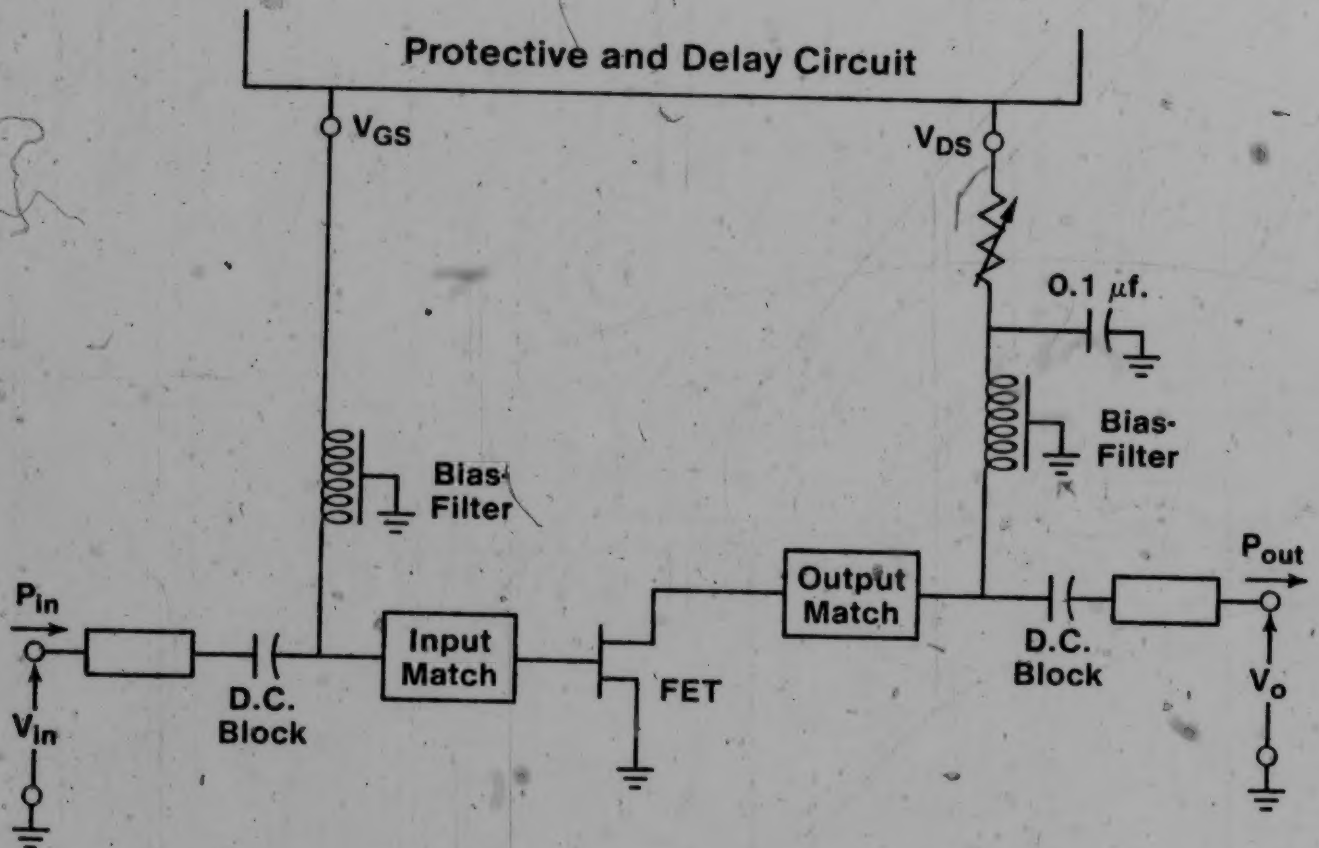
Protective and Delay Circuit
V_{GS}
V_{DS}
0.1 µf.
Bias-Filter
Bias-Filter
P_{in}
V_{in}
D.C. Block
Input Match
FET
Output Match
D.C. Block
P_{out}
V_o

Fig. 4.1 A Schematic Diagram of the GaAs FET Amplifier Configuration

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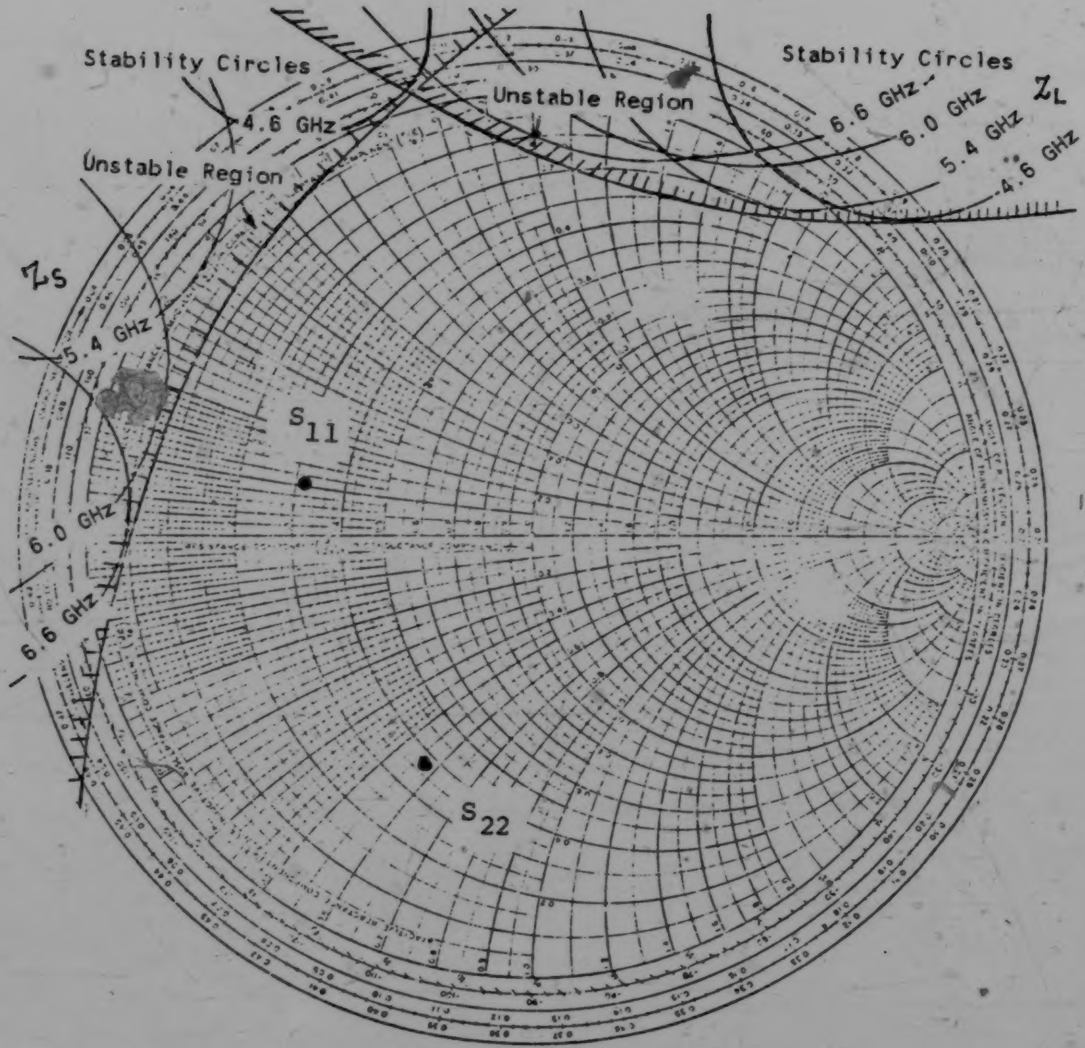


Fig. 4.2 Regions of Instability Plotted on a Smith Chart; Device HP-HFET-1101, $V_{DS} = 3.0V$, $V_{GS} = -1.0V$

The source and load terminations should be selected such that they lie in the stable region of the Smith Chart, at all operating bias potentials of the device. Once an initial selection was made for the matching circuits, the overall amplifier response was modeled by using the computer programme COMPACT. The modeled parameter values for the connector discontinuities and the coaxial-to-microstrip transitions, as listed in Table 3.2, were included in the model. The designed matching circuit dimensions could be altered so as to obtain the desired amplifier response. This design procedure allows predetermination of the amplifier response before the circuit layout is made and the final circuit is etched on the microstrip. Fig 4.3 shows some of the hardware features of the realised amplifier. The aluminum box is used in the bias circuit for shielding of the bias connections from high-frequency noise. The biasing circuit on the substrate consists of a quarter wave length high impedance line (≈ 80 ohm) terminated with a quarter wavelength open circuited low impedance line (≈ 10 ohm). Such an arrangement provides an high RF impedance at the connection with the 50 ohm line. The bias potentials are connected at the interconnecting junction of these two lines by a very thin wire. The bias circuits should be placed far away from the device so that their effect on the amplifier response is minimum.

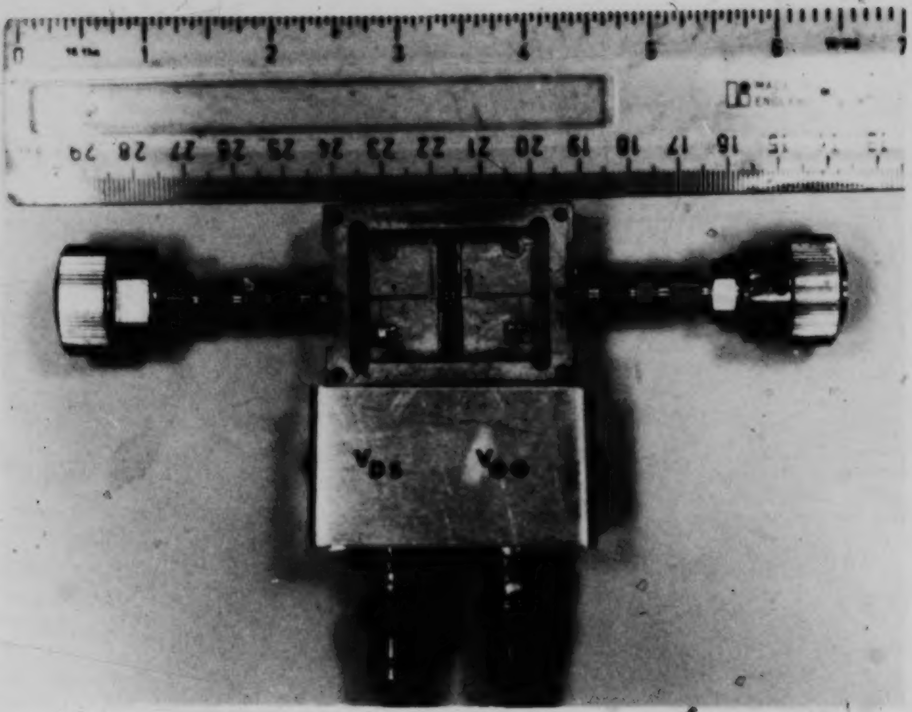


Fig. 4.3 A Photograph of complete 6 GHz GaAs FET Amplifier Assembly

4.4 Modeling of GaAs FET Amplifier Response:

A distributed model for the GaAs FET amplifier is shown in Fig 4.4. The model was simulated with the computer program COMPACT. This model allows computation of the overall magnitude and phase response of the amplifier between its external ports P_a and Q_a respectively. The model is complete in that it includes the device parameters, the matching circuits, all the line lengths, line losses, connector discontinuities and the transitions. The modeled response closely followed the measured amplifier gain and phase response except that the center frequency was observed to be shifted by approximately 100 MHz. Such a shift occurs because the end effects of the matching stubs are not included in the model. To complete the amplifier modeling, therefore, another optimisation run was made and the amplifier response was least-square-fitted to the measured amplifier response. The final values of the stub lengths are listed in Table 3.2. Fig. 4.5 shows the comparison between modeled and measured amplifier gain response. The agreement between measured and modeled gain is observed to be within 1-dB over a frequency range extending over 2 GHz. It is observed that for a given matching network the gain of the amplifier decreases and the bandwidth increases as the gate-bias is made more negative. For a V_{GS} of -1.0 V the center frequency gain is 9.2 dB and 1-dB bandwidth is observed to be approximately 700 MHz. The agreement between measured and modeled phase is observed to be within 30

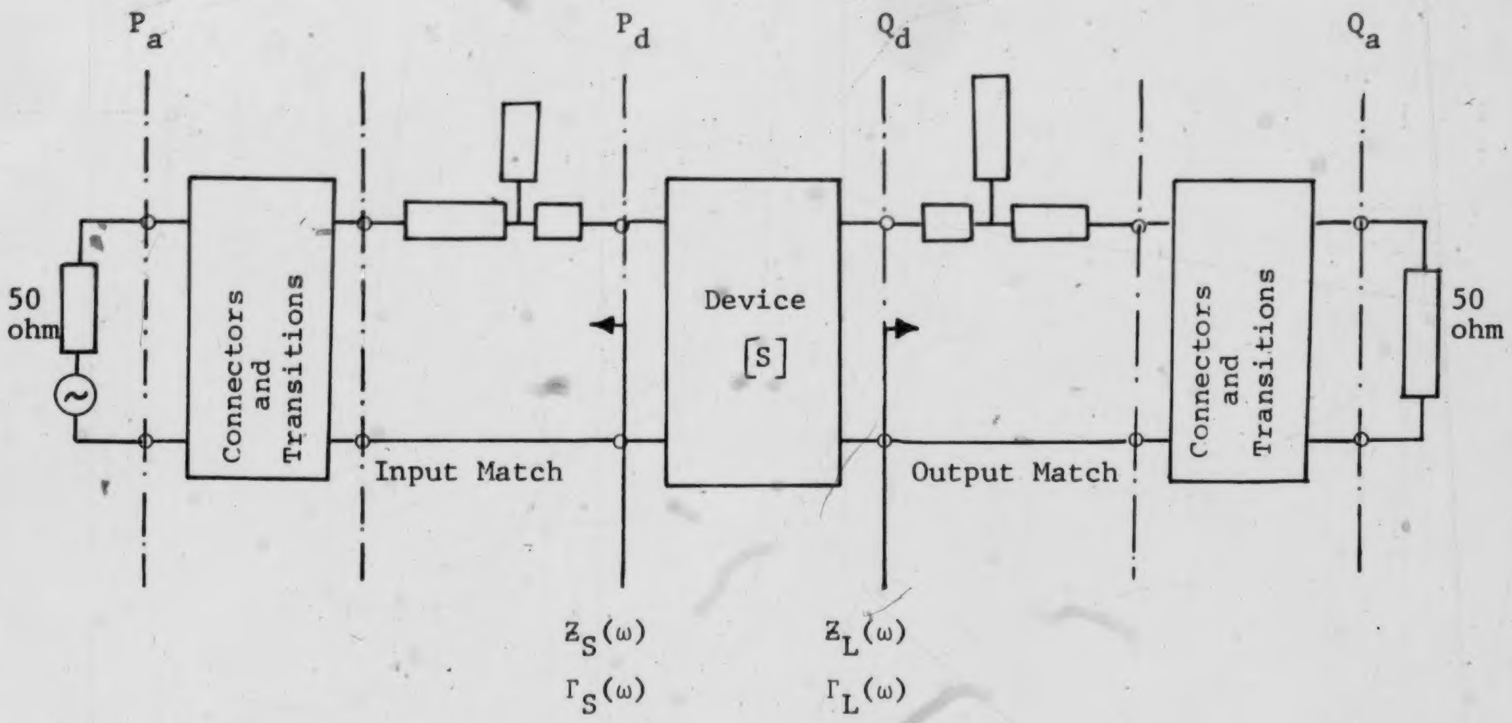

P_a
P_d
Q_d
Q_a
50 ohm
Connectors and Transitions
Input Match
Device
[S]
Output Match
Connectors and Transitions
50 ohm
$Z_S(\omega)$
$\Gamma_S(\omega)$
$Z_L(\omega)$
$\Gamma_L(\omega)$

Fig. 4.4 A Distributed Model for the GaAs FET Amplifier

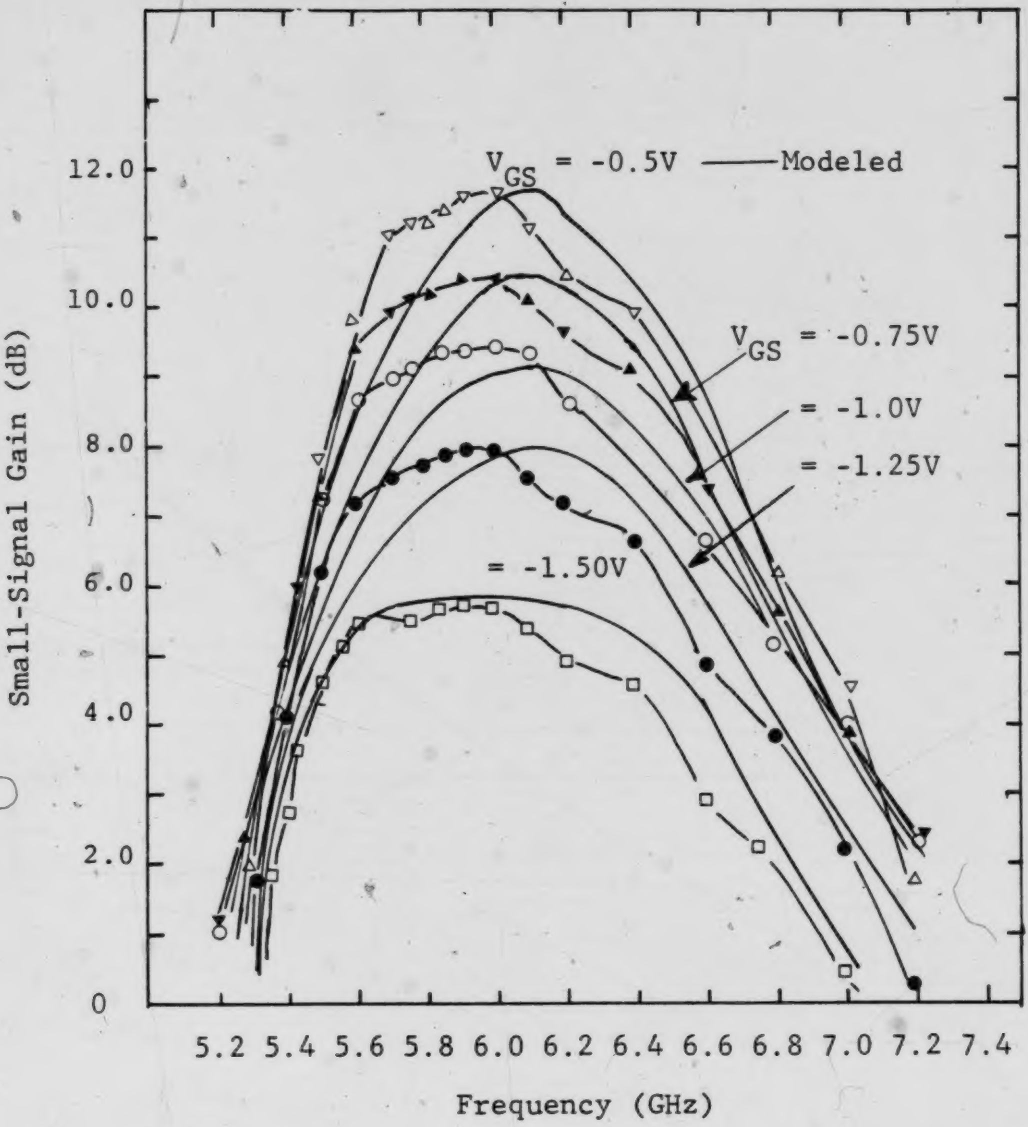


Fig. 4.5 Modeled and Measured Small-Signal Gain of the GaAs FET Amplifier as a Function of Frequency at Several Gate-Bias Voltages

degrees over a 1 GHz amplifier bandwidth. The comparison is shown in Figure 4.6.

The measurements of the amplifier gain and phase response were obtained by using the network analyzer measurement set-up described in section 3.4. The network analyzer allows a swept frequency display of the forward gain parameter of the amplifier. For improved accuracy, however, the measurements were carried out at discrete frequencies in the amplifier pass band. The analysis of the amplifier response at various gate-bias voltages indicated that the amplifier tends to be unstable at less negative bias voltages. S_{11} was observed to be greater than unity for a gate bias of -0.1 V, an unstable condition for amplifier operation. It is essential to operate the amplifier far away from this region of instability so that any change in device parameters due to temperature changes or due to larger input signal strength will not cause the amplifier to oscillate. Therefore, the operation of the amplifier was restricted to gate voltages less than -0.5 volts.

The good agreement obtained between measured and modeled amplifier response underlines the importance of the method of characterisation and modeling of the overall amplifier response developed in Chapter III and chapter IV. Two amplifiers were designed, using devices from different manufacturers (HP HFET-1101 and NEC-24406 devices) and good agreement was obtained in both cases. The results presented in this chapter and the next chapters refer to the HP HFET-1101 device.

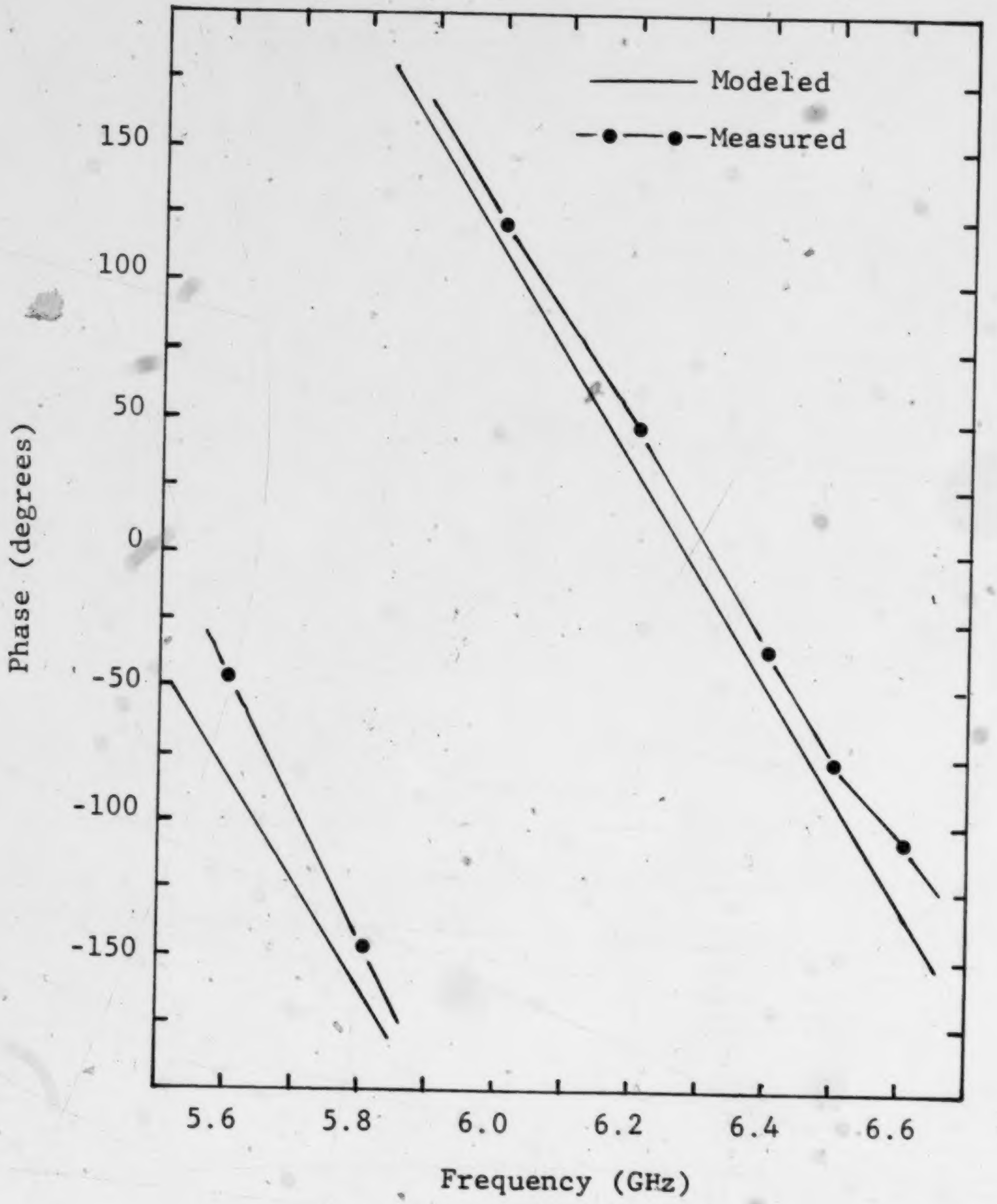


Fig. 4.6 Modeled and Measured Phase of the Overall GaAs FET Amplifier, as a Function of Frequency; Device HP HFET-1101, V_{DS} = 3.0V, V_{GS} = -1.0V

CHAPTER V

DISTORTION ANALYSIS OF THE GaAs FET AMPLIFIER USING VOLTERRA SERIES REPRESENTATION

In this chapter, a mathematical model is developed to study the amplitude and phase nonlinearities observed in the GaAs FET amplifier. A frequency-domain Volterra-series expansion has been used as the analysis technique. For purposes of analysis, a lumped circuit model is proposed for the overall amplifier. One of the significant features of the model is that it takes into account the device nonlinearities and their interaction with the surrounding microwave circuit. The microwave circuit is taken to consist of the matching circuits, the coaxial-to-microstrip transitions and the discontinuities associated with the input connectors and dc blocking capacitors. The distortion in the amplifier is investigated as a function of input signal power level, signal frequency and transistor gate-bias. A gate-bias compensation technique is described to improve the distortion performance of the amplifier.

5.1 Introduction

Intermodulation and cross modulation are important measures of amplifier distortion. The process of generation of spurious responses within an amplifier's passband, when a number of signals are applied to the amplifier input, is called intermodulation distortion. The third-order intermodulation product is of particular importance, since it lies nearest to the signal frequencies and therefore dominates the distortion. Further, the fundamental component of the third-order term contributes significantly towards the power level-dependent amplitude- and phase nonlinearities of the amplifier's response. Cross modulation distortion is defined as the transfer of modulation from one carrier to another when a number of amplitude-modulated signals are applied to the amplifier input.

At low frequencies, the transfer characteristics of an amplifier can be expressed as a power series, and the distortion performance is readily calculated. Power-series expansion analysis applies only to nonlinear zero-memory circuits, for which the output at any time 't' depends only on the input at the same time instant. The microwave amplifier model includes, however, package inductances and fringe capacitances and nonlinear reactive elements associated with the device model. These nonlinear energy-storage (memory) elements produce frequency dependent distortion. The transfer characteristics of such an amplifier with memory can be represented by a Volterra-series. Volterra-series coefficients (kernels) are frequency dependent and contain the phase information. Therefore, the Volterra series representation is suitable for computing the response of nonlinear circuits with memory.

5.2 Review of Volterra-series

A sufficient condition that the Volterra-series analysis may be applied to the GaAs FET amplifier is that the operation of the amplifier must be restricted to a region of asymptotic stability. The concept of Volterra functionals in the analysis of nonlinear systems is a generalization of the convolution integral used in linear system analysis. All possible input functions x(t) are transformed to a set of output functions y(t), through Volterra series integrals, which define the system transfer function. The Volterra-series may be described as a 'power-series with memory' which expresses the output of a nonlinear system in 'powers' of the input x(t). The output depends on the past values of the input; therefore, the nth order Volterra integral involves expressions with products of input with itself, thus representing an nth order system.

Volterra showed that every functional y(t) continuous in the field of continuous functions can be represented by the expansion [50]

$$v(t) = \sum_{k=1}^{\infty} y_k(t) \tag{5.1}$$

where y_k is a homogeneous functional of order k and has the form

$$y_k(t) = \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \cdots\cdots \int_{-\infty}^{\infty} h_k(\tau_1, \tau_2, \ldots., \tau_k).x(t-\tau_1).x(t-\tau_2)\ldots.$$

$$.x(t-\tau_k).\ d\tau_1.d\tau_2.d\tau_3.\ldots\ldots.d\tau_k \tag{5.2}$$

The series is called convergent if a definite value of the functional corresponds to every function x(t). For a convergent series, the higher-order functionals can be normally ignored in the analysis as long as the nonlinearities are not too 'violent'. The output y(t) of a nonlinear system can be represented in terms of x(t) as

$$
\begin{aligned}
y(t) = & \int_{-\infty}^{\infty} h_1(\tau_1).x(t-\tau_1).d\tau_1 \\
& + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_2(\tau_1,\tau_2).x(t-\tau_1).x(t-\tau_2).d\tau_1.d\tau_2 \\
& + \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_3(\tau_1,\tau_2,\tau_3).x(t-\tau_1).x(t-\tau_2).x(t-\tau_3). \\
& \qquad d\tau_1.d\tau_2.d\tau_3 \\
& + \ldots\ldots\ldots\ldots + \ldots\ldots\ldots\ldots \qquad (5.3)
\end{aligned}
$$

where $h_k\ (\tau_1,\tau_2,....,\tau_k)$ is the kth kernel of the Volterra expansion of y(t) in terms of x(t). It is assumed here that h_k is a symmetrical function of its arguments. The kth order Fourier transform of $h_k\ (\tau_1,\tau_2,....,\tau_k)$ can be obtained from

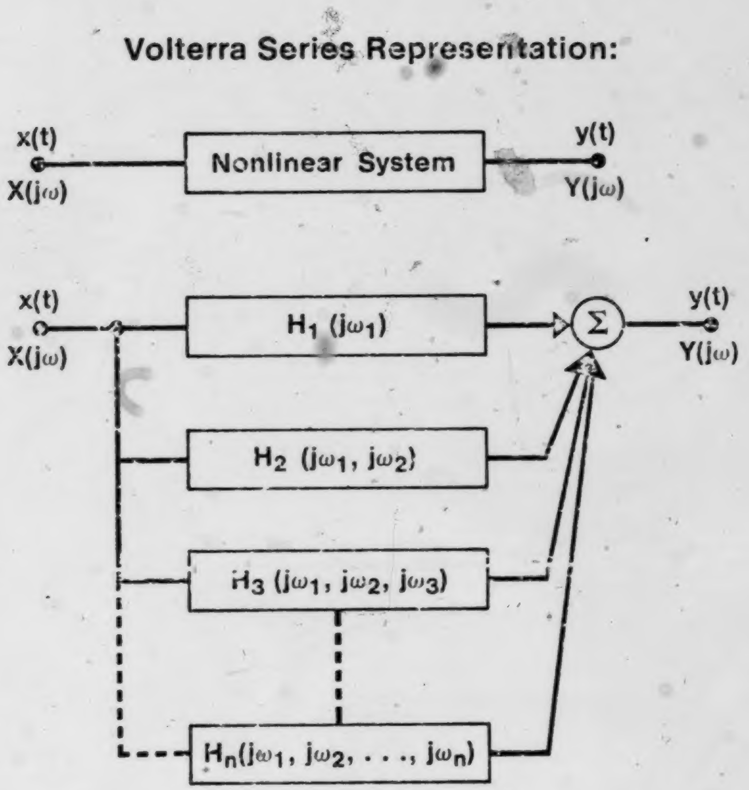
$$
\begin{aligned}
H_k(\omega_1,\omega_2,....,\omega_n) = & \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} h_k(\tau_1,\tau_2,....,\tau_k). \\
& \exp[-j(\omega_1\tau_1+\omega_2\tau_2+\ ....\omega_k\tau_k)]d\tau_1.d\tau_2,....,d\tau_k
\end{aligned}
$$

$$(5.4)$$

where $\omega_k = 2\pi f_k$ and H_k is also a symmetrical functions of its arguments. The order of H_k can be thought of as the number of contributing input frequencies when the input is sum of individual tones. In general, different order nonlinearities result in responses at the same frequency in nonlinear systems. An arbitrary nonlinear system is represented as a sequence of systems connected in parallel as shown in Fig 5.1.

The Volterra series expansion leads to an infinite number of terms; however, the first few terms of the series suffice as long as the amplifier is operated in the region of mild nonlinearities. Therefore, the analysis described in this thesis is applicable mainly in the current saturation region of device operation. Furthermore, the gate drive is considered to be small so that a) the distortion is small, b) the quasi-linear approximation of the device model remains valid, and c) the dc component at the output of the amplifier does not change the operating conditions of the device.

The application of the Volterra functionals to the analysis of nonlinear circuits was originally suggested by Wiener[50]. Therefore, Volterra kernels are also sometimes referred as Volterra-Wiener kernels. In 1967, Narayanan [51] first applied the technique to distortion analysis of a bipolar transistor amplifier operating at 20 MHz. Since the Volterra-series approach gives an explicit input/output relationship in terms of functionals, it was extended for


Volterra Series Representation:
x(t)
X(jω)
Nonlinear System
y(t)
Y(jω)
x(t)
X(jω)
$H_1(j\omega_1)$
Σ
y(t)
Y(jω)
$H_2(j\omega_1, j\omega_2)$
$H_3(j\omega_1, j\omega_2, j\omega_3)$
$H_n(j\omega_1, j\omega_2, \ldots, j\omega_n)$

$$Y(j\omega) = \sum_{n=1}^{\infty} Y_n(j\omega_1, j\omega_2, \ldots, j\omega_n)$$

$$Y_n(j\omega_1, j\omega_2, \ldots, j\omega_n) = H_n(j\omega_1, j\omega_2, \ldots, j\omega_n) \prod_{i=1}^{n} x(j\omega_i)$$

Fig. 5.1 Volterra-Series Representation of a Nonlinear System

application to a large class of amplifiers. Narayanan extended his work to analyze distortion in cascaded and feedback amplifiers [52]. Narayanan and Poon [53] used the Volterra series expansion technique for third-order amplifier distortion studies of a bipolar transistor using the integral charge control model. Van Trees[54] applied the analysis to study the nonlinear behavior of phase locked loops. Cross modulation and intermodulation in 100 MHz transistor amplifiers were investigated by Meyer et al. [55] using the Volterra-series approach. Khader and Johnson [56] applied the technique for distortion analysis of a 10 MHz FET amplifier. At microwave frequencies the technique has been extended for the distortion analysis of reflection-type IMPATT amplifiers [57]. More recently, it has been used to study the second-order [58] and third-order harmonic distortion of a microwave MESFET mounted in a 50 ohm transmission system. In a significant paper, Bussgang et al. [59] applied the technique to a distortion analysis of communication receivers. The paper sums up the available techniques for the analysis of nonlinear systems using Volterra series expansion. Bedrosian and Rice [60] have given an excellent review of the analysis of nonlinear systems with memory driven by harmonic and Gaussian inputs.

5.3 Distortion Analysis of the GaAs FET Amplifier

In this thesis, the nonlinear transfer functions of the GaAs FET amplifier are determined by the nonlinear current method [60] and network analysis. The accuracy of the analysis, therefore, depends upon the accuracy with which these nonlinear currents can be determined and the accuracy and validity of the amplifier model. The active device contains more than one nonlinearity, and the distortion currents are dependent upon the potentials and their derivatives across each nonlinearity. The transfer functions are computed recursively; by first computing the linear kernels and then estimating the higher order kernels. The analysis procedure involves the following steps:

a) Derivation of a suitable amplifier model and identification of the dominant device nonlinearities. The nonlinear model is treated essentially as a linear network, with nonlinearities superimposed upon it.

b) The linear transfer function is computed by considering all the circuit elements as linear.

c) The higher-order distortion currents are computed from a knowledge of the linear potentials and the coefficients of the expanded Taylor Series. These higher-order distortion currents are treated as input signals, the external voltage sources are assumed to be short circuited and higher-order nodal voltages are computed.

From the higher order nodal voltages, the distortion levels in the amplifier can be studied as a function of various parameters extrinsic to the device.

5.3.1 Nonlinear Amplifier Model

A good model is a simple but realistic representation of a physical phenomenon in terms of measurable parameters such that the phenomenon can be analyzed and controlled, if possible. The distributed amplifier model discussed in Section 4.3 is not suitable for nonlinear analysis of the amplifier because no explicit information is available regarding internal potentials within the active device. A lumped circuit model is developed in this section for Volterra-series analysis of the amplfier. The model, shown in Figure 5.2, includes a device model, its nonlinearities and their interaction with the surrounding microwave circuit. The device model is derived by the method described in section 3.4 and includes the effect of feedback elements such as the drain-gate Miller capacitance C_{dg} , the source resistance R_s and inductance L_s . In Figure 5.2, the reference planes P_a and Q_a refer to the external ports of the amplifier, and P_d and Q_d refer to the device ports. The intermediate network consists of the matching circuits, coaxial-to-microstrip transitions, and the discontinuities associated with the coaxial connectors and dc blocking capacitors. Z_S and Z_L refer to the source and load impedances as seen by the device at its gate and drain

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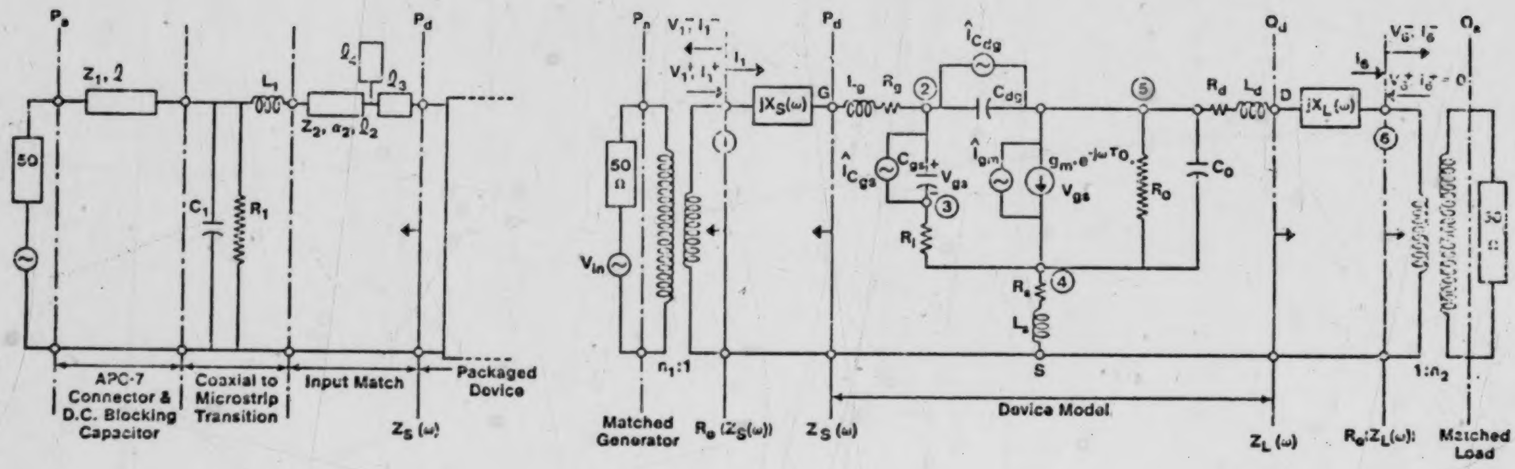
P_e
Z_1, ℓ
50
L_1
C_1
R_1
Z_2, α_2, ℓ_2
ℓ_4
ℓ_3
P_d
APC-7 Connector & D.C. Blocking Capacitor
Coaxial to Microstrip Transition
Input Match
Packaged Device
$Z_S(\omega)$
P_n
50 Ω
V_{in}
$n_1:1$
Matched Generator
V_1^-, I_1^-
V_1^+, I_1^+
I_1
①
$jX_S(\omega)$
G
$R_e(Z_S(\omega))$
$Z_S(\omega)$
L_g
R_g
②
$\hat{i}_{Cdg}$
C_{dg}
$\hat{i}_{Cgs}$
C_{gs}
V_{gs}
③
R_i
$\hat{i}_{gm}$
$g_m \cdot e^{-j\omega\tau_0} \cdot V_{gs}$
④
R_s
L_s
S
⑤
R_0
C_0
R_d
L_d
D
Device Model
O_d
$Z_L(\omega)$
$jX_L(\omega)$
I_6
V_6^-, I_6^-
$V_6^+, I_6^+ = 0$
⑥
$R_e(Z_L(\omega))$
$1:n_2$
50 Ω
O_e
Matched Load

(a) (b)

Fig. 5.2 A Nonlinear Lumped Circuit Model for the GaAs FET Amplifier

ports, respectively. The complex values of Z_S and Z_L can be computed at various frequencies from the design values of the matching circuits and the characterised values of the remaining intermediate networks. The computed values are plotted on a Smith Chart as a function of frequency in Figure 5.3 . Power transfer is assumed to take place across ideal lossless transformers with turns ratios n_1 and n_2 , at the input and output of the amplifier respectively. Typically, the losses at the amplifier input and output are about 0.3-0.5 dB at each port and can therefore be ignored in the analysis. The equivalent lengths of the transmission lines at the ports P_a and Q_a are not included in the model. These lengths cause only a linear phase shift in the overall response of the amplifier and do not influence the nonlinear response of the amplifier during analysis. The matched generator and matched load are taken to mean that there are no multiple reflections at the input and output port of the amplifier. That is, it is assumed that the amplifier is coupled through ideal circulators or isolators at the input and output ports of the amplifier. The terms $\hat{i}_{C_{gs}}$, $\hat{i}_{C_{dg}}$ and $\hat{i}_{g_m}$ represent the small nonlinear distortion currents which are superimposed upon the linear circuit currents. These currents are estimated from the device nonlinearities obtained during the characterisation and modeling process described in Chapter III. The dominant nonlinearities that produce the distortion currents are described in the next Section.

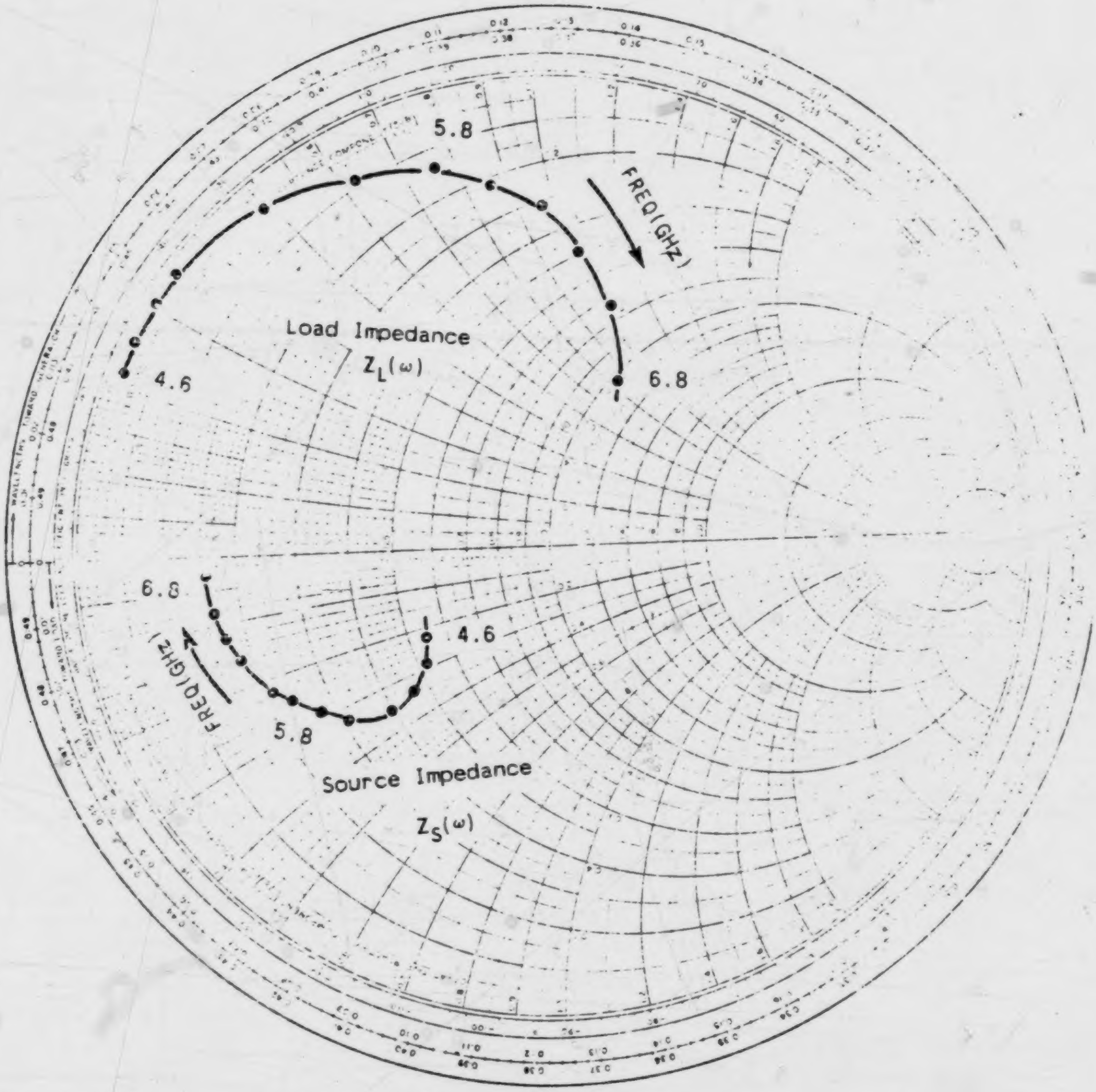

Fig. 5.3 Source and Load Impedances of the GaAs FET Amplifier, as a Function of Frequency

5.3.2 Device Nonlinearities:

The bias dependence of the nonlinear intrinsic elements in the device was obtained by least-square fitting the device model to the measured S-parameters at various gate and drain bias voltages. The bias dependence of the nonlinear circuit elements of the FET was observed to be similar to that expected from device physics relationships. The output resistance R_o was observed to be almost constant as a function of the gate voltage over the operating range of interest (current-saturation region of the device operation), but linearly dependent on the drain voltage V_{DS}. Since the output resistance is not directly a part of the FET gain mechanism, its contribution to the intermodulation distortion will be small [61]. An averaged value of R_o was therefore used. Analytical expressions for the nonlinear device parameters g_m, C_{gs} [22], and an empirical relation for C_{dg} were curve-fitted to the measured data.

a) Transconductance Nonlinearity

For constant V_{DS}, a simple relation for the drain current as a function of gate-bias is described in Section 2.2. Equation (2.19) may be rewritten as

$$I_d = I_{dss}\left[1 - \left(\frac{V_{SG} + \phi}{W_{oo}}\right)\right]^{1/2} \tag{5.5}$$

where ϕ is the Schottky-barrier contact potential (ϕ =0.8V), and W_{oo} is the pinch-off potential. The Taylor series expansion of the above expression is

$$i_d = g_{m_1} \cdot v_{gs} \cdot e^{j\omega(t-\tau_1)} + g_{m_2} \cdot v_{gs}^2 \cdot e^{j\omega(t-\tau_2)} + g_{m_3} \cdot v_{gs}^3 \cdot e^{j\omega(t-\tau_3)} + \ldots\ldots \qquad (5.6)$$

where i_d and v_{gs} are small a.c. current and voltage components. g_{m_1} , g_{m_2} and g_{m_3} are the coefficients of the Taylor expansion of (5.5). τ_1, τ_2, τ_3 are the order dependent time delays. Higher-order delays are ignored and an averaged value of the delay $\tau_1 = \tau_o$ is used [62]. The corresponding expression for the transconductance is

$$g_m = - \frac{\partial I_d}{\partial v_{sg}} \Bigg|_{\substack{V_{GS}, V_{DS} \\ \text{constant}}} = \frac{I_{dss}}{2\sqrt{W_{oo}}} \left(\frac{1}{V_{SG} + \phi} \right)^{1/2} \qquad (5.7)$$

For a fitted value of I_{dss} = 149.16 mA, the comparison between measured and modeled transconductance is shown in Fig 5.4(a).

Equation (5.5) is based on the gradual channel approximation (GCA) which has been discussed in Chapter II. For submicron gate-length devices this approximation may not be valid. In this case the Taylor series coefficients in equation (5.6) could be obtained by least square fitting a polynomial to the measured transconductance data.

b)Gate-Capacitance Nonlinearity:

For a fixed V_{DS} , from equation (2.24) C_{gs} may be related to V_{SG} as

$$C_{gs} = C_o + C_1 \left(\frac{W_{oo}}{V_{SG}+\phi} \right)^{1/2} \tag{5.8}$$

The corresponding power series expansion is given by

$$i_{Cgs} = C_{gs_1} \frac{\partial v_{gs}}{\partial t} + C_{gs_2} \frac{\partial^2 v_{gs}}{\partial t^2} + C_{gs_3} \frac{\partial^3 v_{gs}}{\partial t^3} + \ldots \tag{5.9}$$

By curve fitting (5.8) to the measured data, we obtain C_o =0.16 pF and C_1 =0.2955 pF. A comparison between modeled and measured values of C_{gs} is shown in Fig 5.4(b).

c)Drain-Capacitance Nonlinearity:

Since no simple relationship is available to model the dependence of C_{dg} on V_{DG} , an empirical relationship was curve fitted to the measured data. For a given value of V_{GS} and V_{DG} , V_{DG} was obtained from $V_{DG} = V_{DS} + V_{SG} + \phi$. The fitted expression is

$$C_{dg} = 0.0514\ (V_{DG} - 3.18)^{1/3} \tag{5.10}$$

The comparison between measured and modeled C_{dg} is shown in Fig 5.4(c). The power series expansion is given by

$$i_{C_{dg}} = C_{dg_1} \frac{\partial v_{dg}}{\partial t} + C_{dg_2} \frac{\partial^2 v_{dg}}{\partial t^2} + C_{dg_3} \frac{\partial^3 v_{dg}}{\partial t^3} + \ldots. \tag{5.11}$$

Since the nonlinearities are small, the series is truncated after three terms. For amplifiers with less than an octave bandwidth, such as the FET amplifier considered here, even-order terms produce distortion products which fall outside the amplifier band[62]. Any difference frequency terms obtained from the two-tone signal see a short circuit in the output, because of the 0.1 μf capacitor in the bias circuit (see Fig. 4.1).

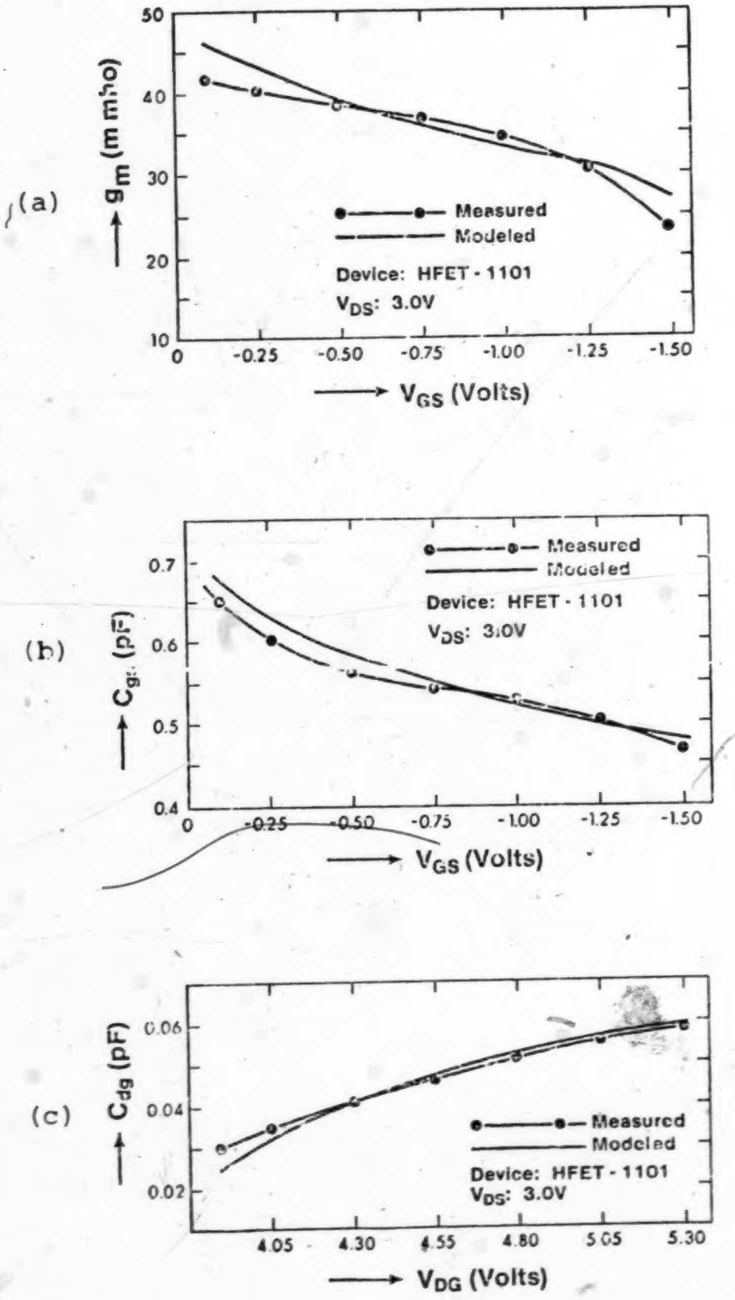

Fig. 5.4 Comparison of the Measured and Modeled Bias Dependence of Nonlinear Elements

(a) Transconductance g_m

(b) Gate-to-Source Capacitance C_{gs}

(c) Drain-to-Gate Capacitance C_{dg}

Therefore, the second-order terms in (5.7), (5.9) and (5.11) are ignored. The third-order nonlinear coefficients of the expansion for V_{DS} =3.0V and V_{GS} =-1.0V were computed to be C_{gs_3}=-0.01422 pF/V^2, g_{m_3} =1.2817 m mho/V^2 and C_{dg_3}=0.00190 pF/V^2 .

5.3.3 Volterra Series Analysis

Six nodes are defined for the overall amplifier equivalent circuit (Fig 5.2). Nodes 1 and 6 are 'virtual nodes' that cannot be physically located on the distributed input and output circuits. These nodes are defined purely from power transfer considerations across the frequency dependent real parts of the complex source and load impedances. The imaginary parts of these impedances therefore is lumped together with the device model. The frequency dependence of the real and imaginary parts of the source and load impedances is shown in Figures 5.5(a) and 5.5(b). The symbols v_1^+ , i_1^+ and v_1^- , i_1^- are the equivalent voltage and current components of the incident and reflected waves at node 1; i_1 represents the net current flowing into the gate circuit of the transistor and v_1 is the terminal voltage at node 1. These voltages and currents are related by

$$v_1 = v_1^+ + v_1^- \qquad (5.12)$$

$$i_1 = i_1^+ - i_1^- \qquad (5.13)$$

Therefore

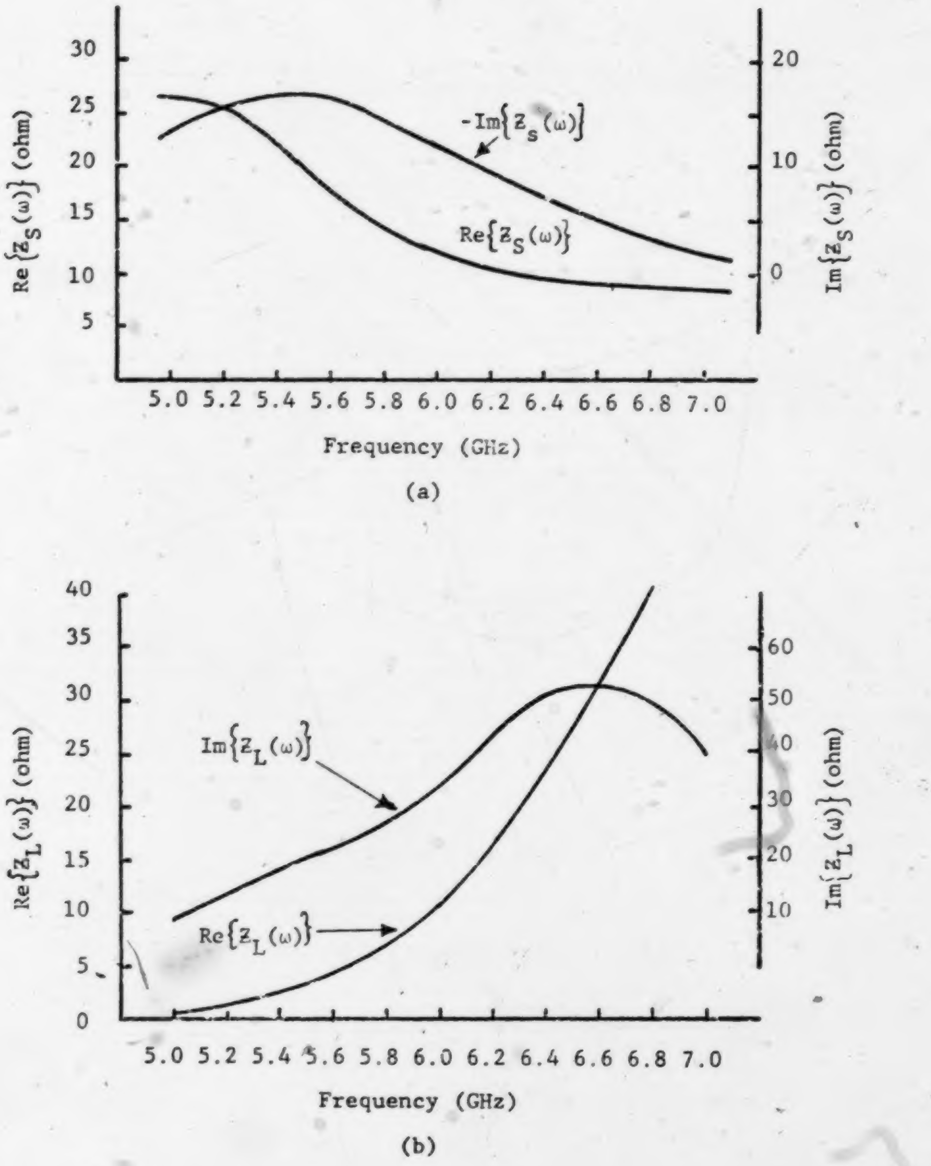

Fig. 5.5 Real and Imaginary Parts of Source and Load Impedances as a Function of Frequency

(a) Source Impedance

(b) Load Impedance

$$i_1 = \frac{1}{R_e\{Z_S(\omega)\}} [2v_1^+ - v_1] \qquad (5.14)$$

The symbols v_6^+, i_6^+, v_6^-, i_6^-, and v_6, i_6 refer to the corresponding voltages and currents at node 6. Since a perfectly matched termination has been assumed, v_6^+ and i_6^+ will both be zero. Therefore, the terminal voltage and current v_6 and i_6 are related by

$$i_6 = i_6^- = \frac{v_6^-}{R_e\{Z_L(\omega)\}} = \frac{v_6}{R_e\{Z_L(\omega)\}} \qquad (5.15)$$

v_1^+ and v_6^- are related to the equivalent input and output voltages V_{in} and V_{out} through frequency-dependent transformer ratios n_1 and n_2

$$v_{in} = n_1 v_1^+ \qquad (5.16)$$

$$v_{out} = n_2 v_6^- \qquad (5.17)$$

where

$$n_1 = \sqrt{\frac{Z_o}{R_e\{Z_s(\omega)\}}} \quad \text{and} \quad n_2 = \sqrt{\frac{Z_o}{R_e\{Z_L(\omega)\}}} \qquad (5.18)$$

Using (5.14) and (5.15), a set of nodal equations may be derived for the overall circuit by applying Kirchoff's current law at each node. Nonlinear currents are included as frequency and voltage-dependent current sources. The following set of equations results

$$\left[\frac{1}{R_e\{Z_S(\omega)\}} + \frac{1}{R_g+jX_S(\omega)+j\omega L_g}\right] v_1 - \left[\frac{1}{R_g+j\omega L_g+jX_S(\omega)}\right] v_2$$

$$= \frac{2v_1^+}{R_e\{Z_S(\omega)\}} \qquad (5.19)$$

$$\left[\frac{1}{R_g+j\omega L_g+jX_s(\omega)}\right] v_1 + \left[\frac{1}{R_g+j\omega L_g+jX_S(\omega)} + j\omega C_{gs} + j\omega C_{dg}\right] v_2$$

$$- j\omega C_{gs}\cdot v_3 - j\omega C_{dg}\cdot v_6 + \hat{i}_{C_{gs}}(v_2-v_3) - \hat{i}_{C_{dg}}(v_5-v_2) = 0$$

$$(5.20)$$

$$- j\omega C_{gs}\cdot v_2 + [\frac{1}{R_i} + j\omega C_{gs}]\cdot v_3 - \frac{1}{R_i} v_4 - \hat{i}_{C_{gs}}(v_2-v_3) = 0$$

$$(5.21)$$

$$- [g_m\cdot e^{-j\omega\tau_o}]v_2 + [g_m e^{-j\omega\tau_o} - \frac{1}{R_i}]v_3 + [\frac{1}{R_i} + \frac{1}{R_o} + j\omega C_o + \frac{1}{R_s+j\omega L_s}]v_4$$

$$- [\frac{1}{R_o} + j\omega C_o]v_5 - \hat{i}_{g_m}(v_2-v_3) = 0 \qquad (5.22)$$

$$[g_m e^{-j\omega\tau_o} - j\omega C_{dg}']v_2 - g_m e^{-j\omega\tau_o} v_3 - [\frac{1}{R_o} + j\omega C_o]v_4$$

$$+ (\frac{1}{R_d+j\omega L_d+jX_L(\omega)} + j\omega C_{dg} + j\omega C_o + \frac{1}{R_o})v_5$$

$$- [\frac{1}{R_d+j\omega L_d+jX_L(\omega)}]v_6 + \hat{i}_{C_{dg}}(v_5-v_6) + \hat{i}_{g_m}(v_2-v_3) = 0$$

$$(5.23)$$

$$- [\frac{1}{R_d+j\omega L_d+jX_L(\omega)}]v_5 + [\frac{1}{R_e\{Z_L(\omega)\}} + \frac{1}{R_d+j\omega L_d+jX_L(\omega)}]v_6 = 0$$

$$(5.24)$$

These equations describe the overall amplifier model of Fig 5.2(b). These equations can be written in the following form

$$[A(j\omega)][V_{nm}(j\omega)] + [\text{Distortion Currents}] = [I_{ni}(j\omega)] \tag{5.25}$$

$[A(j\omega)]$ is a six-by-six matrix with complex coefficients, and consists of all linear terms of equations (5.19)-(5.24), and is shown in Figure 5.6 . $V_{nm}(j\omega)$ is the nodal voltage matrix, where n refers to the number of the reference node and m is the order of the Volterra kernel. The estimation of the nodal voltage kernels is done recursively [51], [59]; the first-order kernels are obtained by ignoring the nonlinear currents and solving only the linear terms. By matrix inversion, we obtain

$$[V_{n1}(j\omega)] = [A(j\omega)]^{-1}[I_{1i}(j\omega)] \tag{5.26}$$

where

$$I_{1i}(j\omega) = \begin{bmatrix} \dfrac{2v_1^+}{R_e\{Z_S(\omega)\}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.27}$$

The matrix inversion was obtained using extended precision arithmetic. Some of the matrix elements are much

$$[A(j\omega)] = \begin{bmatrix} \frac{1}{R_e\{Z_S(\omega)\}} + \frac{1}{R_g+j\omega L_g+jX_S(\omega)} & \frac{1}{R_g+j\omega L_g+jX_S(\omega)} & 0 & 0 & 0 & 0 \\ \frac{1}{R_g+j\omega L_g+jX_S(\omega)} & \frac{1}{R_g+j\omega L_g+jX_S(\omega)} + j\omega C_{gs} + j\omega C_{dg} & -j\omega C_{gs} & 0 & -j\omega C_{dg} & 0 \\ 0 & -j\omega C_{gs} & \frac{1}{R_i} + j\omega C_{gs} & -\frac{1}{R_1} & 0 & 0 \\ 0 & -g_m e^{-j\omega\tau_o} & g_m e^{-j\omega\tau_o} - \frac{1}{R_i} & \frac{1}{R_i} + \frac{1}{R_D} + j\omega C_o + \frac{1}{R_S+j\omega L_S} & -(\frac{1}{R_o} + j\omega C_o) & 0 \\ 0 & g_m e^{-j\omega_c\tau} - j\omega C_{gs} & -g_m e^{-j\omega\tau} & -(\frac{1}{R_o} + j\omega C_o) & \frac{1}{R_d+j\omega L_d+j\omega X_L(\omega)} + j\omega C_{dg} + j\omega C_o + \frac{1}{R_o} & -\frac{1}{R_d+j\omega L_d+jX_L(\omega)} \\ 0 & 0 & 0 & 0 & \frac{-1}{R_d+j\omega L_d+jX_L(\omega)} & \begin{array}{c} \frac{1}{R_e\{Z_L(\omega)\}} \\ \frac{1}{R_d+j\omega L_d+jX_L(\omega)} \end{array} \end{bmatrix}$$

Fig. 5.6 A Six-by-Six System Matrix for the Overall Amplifier

smaller than other elements; therefore a high accuracy solution was necessary for this computation step. $V_{n1}(j\omega)$, (n=1 to 6) represent the first-order nodal voltage kernels. Using (5.12) to (5.18) and (5.26), the small-signal gain of the amplifier was computed. The comparison between measured and calculated gain over 1 GHz amplifier bandwidth is shown in Fig. 5.7. It is observed that the measured and modeled gain of the amplifier are in good agreement. The amplifier gain, computed from the lumped circuit model, is more than that calculated from the distributed circuit model of Fig. 4.3. by approximately 0.6 dB. This discrepancy may be attributed to the losses at input and output ports of the amplifier. The second-order kernels are identically zero, since the second-degree terms of the expansion have been ignored.

The third-order kernels are computed by estimating the third-order distortion currents from a knowledge of the linear kernels. These distortion currents are then considered as input signals.

$$\hat{i}_{g_{m3}}(j\omega_1,j\omega_2,j\omega_3) = g_{m3}\prod_{i=1}^{3}(v_{21}(j\omega_i) - v_{31}(j\omega_i)) \tag{5.28}$$

$$\hat{i}_{C_{gs_3}}(j\omega_1,j\omega_2,j\omega_3) = j(\omega_1+\omega_2+\omega_3)C_{gs_3}\prod_{i=1}^{3}(v_{21}(j\omega_i)-v_{31}(j\omega_i)) \tag{5.29}$$

$$\hat{i}_{C_{dg_3}}(j\omega_1,j\omega_2,j\omega_3) = j(\omega_1+\omega_2+\omega_3)\cdot C_{dg_3}\prod_{i=1}^{3}(v_{51}(j\omega_i)-v_{21}(j\omega_i)) \tag{5.30}$$

where

$$v_{n1}(-j\omega_1,-j\omega_2,-j\omega_3) = V^{*}_{n1}(j\omega_1,j\omega_2,j\omega_3) \tag{5.31}$$

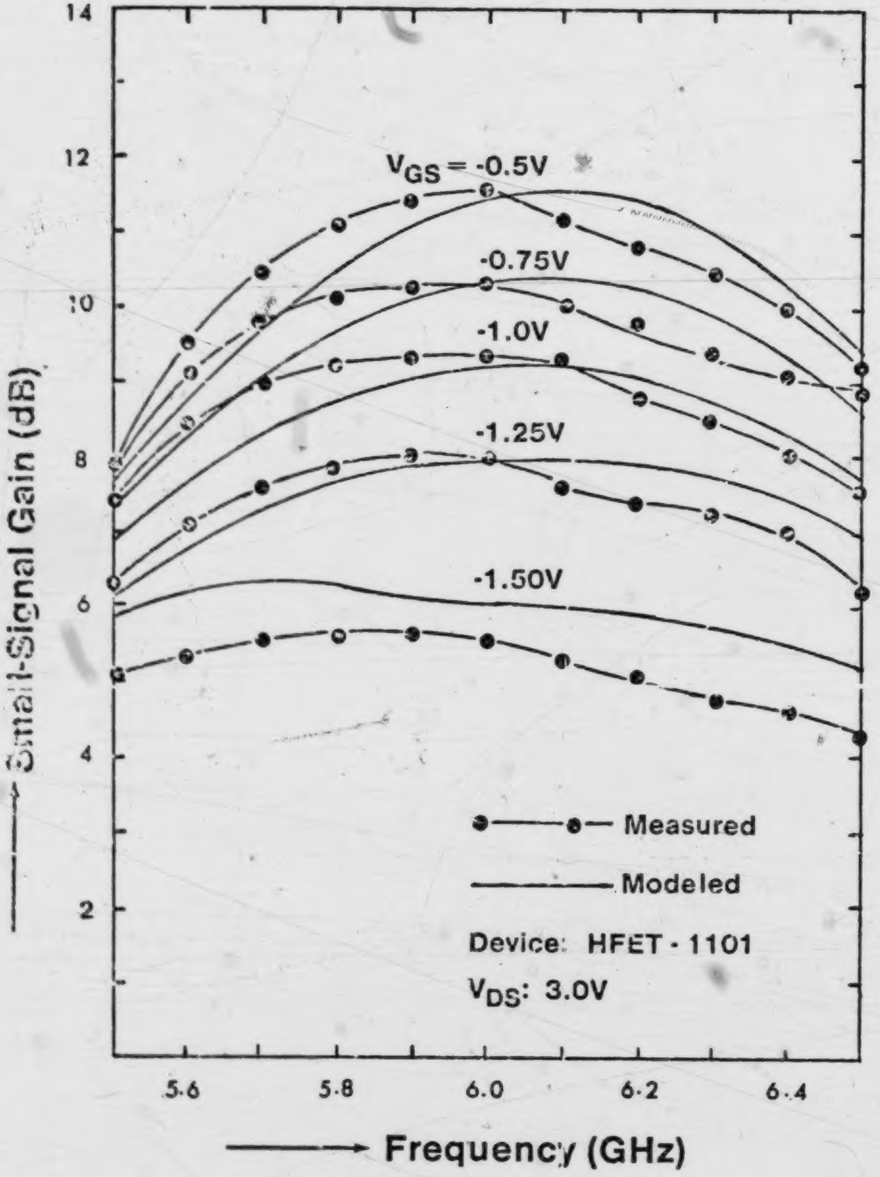

Fig. 5.7 Small-Signal Gain of a GaAs FET Amplifier as a Function of Frequency, at Various Gate-Bias Voltages

and the asterisk indicates the complex conjugate. Third-order kernels are obtained by solving

$$[V_{n3}(j\omega_1,j\omega_2,j\omega_3)] = [A(j\omega_1,j\omega_2,j\omega_3)]^{-1} [I_{31}(j\omega_1,j\omega_2,j\omega_3)] \tag{5.32}$$

where

$$I_{3i} = \begin{bmatrix} 0 \\ -\hat{i}_{C_{gs_3}} + \hat{i}_{C_{dg_3}} \\ \hat{i}_{C_{dg_3}} \\ \hat{i}_{g_{m_3}} \\ -\hat{i}_{C_{dg_3}} - \hat{i}_{g_{m_3}} \\ 0 \end{bmatrix} \tag{5.33}$$

The third-order kernels were numerically evaluated at the frequencies of interest.

5.3.4 Computation of Intermodulation Distortion:

The two-tone test method was used for the computation and experimental measurement of intermodulation distortion in the GaAs FET amplifier. It is well recognised that the reliability of IM testing for system evaluation increases as the probing signal spectrum approaches that of the actual system signal. The three-tone test requires improved filtering and a larger measurement set-up. For characterizing the IM performance of devices or systems however, the two-tone test provides an effective means for device evaluation. Measurements are made at low input power levels and then extrapolated to the large signal region. The output power level where the fundamental and the third-order distortion product are equal in magnitude is defined as the Intercept Point. For third-order nonlinearities, the intercept point P_I provides a convenient standard by which the IM performance of devices may be specified and compared. Care should be exercised to ensure that extrapolation is still valid in the region of larger input power-levels. It has, for example, been pointed out by Strid and Duder[63] that, for certain power GaAs FETs, the intermodulation distortion product is ill-behaved and the concept of the intercept point does not hold. However, for low-noise low power GaAs FETs it has been found that the intermodulation distortion behavior follows the expected 3:1 slope and is largely well-behaved[64].

For a two-tone intermodulation distortion test [62], the amplifier was excited by an input signal of the form

$$V_{in} = V \cos\omega_1 t + V \cos\omega_2 t \qquad (5.34)$$

where $\omega_1$and $\omega_2$are incommensurate, and close to each other. The inband third-order intermodulation products will appear at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. Equation (5.35) may be rewritten in the following form

$$V_{in}(t) = \frac{V}{2}\{\exp(j\omega_1 t) + \exp(j\omega_2 t) + \text{C.C.}\} \qquad (5.35)$$

The steady state response at the output at frequency

$2\omega_1 - \omega_2$ is given by

$$y_{2\omega_2-\omega_1} = \frac{1}{8}[V_{o_3}(j\omega_1,j\omega_1,-j\omega_2) + V_{o_3}(-j\omega_2,j\omega_1,j\omega_1) + V_{o_3}(j\omega_1,-j\omega_2,j\omega_1)].\exp[j(2\omega_1-\omega_2)t] + \text{C.C.}] \tag{5.36}$$

$$= \frac{3}{8}[V_{o_3}(j\omega_1,j\omega_1,-j\omega_2).\exp(j(2\omega_1-\omega_2)t) + \text{C.C.}] \tag{5.37}$$

where, CC represents a complex conjugate. Taking only the real parts in the above equations,

$$y_{2\omega_1-\omega_2} = \frac{3}{4}[|V_{o_3}(j\omega_1,j\omega_1,-j\omega_2)|\cos[(2\omega_1-\omega_2)t + \angle V_{o_3}(j\omega_1,j\omega_1,-j\omega_2)]] \tag{5.38}$$

The output at the fundamental frequency ω_2 will be given by

$$y_{\omega_2} = \frac{1}{2}[V_{o_1}(j\omega_2).\exp(j\omega_2) + \text{C.C.}]$$

$$= |V_{o_1}(j\omega_2)|\cos(\omega_2 t + \angle V_{o_1}(j\omega_2 t)] \tag{5.39}$$

The third-order intermodulation distortion is given by the ratio of third-order component to the first-order component

$$IM_3(\text{dB}) = 20\log_{10} \frac{|V_{o_3}(j\omega_1,j\omega_1,-j\omega_2)|}{|V_{o_1}(j\omega_2)|} \tag{5.40}$$

where $V_{o_n}(j\omega_1, j\omega_2, \ldots, j\omega_n)$ is the nth order kernel of the amplifier output voltage at the angular frequency $(\omega_1+\omega_2+\ldots\ldots+\omega_n)$.

In the expression above the contributions from the higher order products, which become significant at larger input levels, have been ignored. Since the two test tones are close to each other $(\omega_1=\omega_2)$, it is assumed that

$$Z_S(\omega_1) \simeq Z_S(\omega_2) \tag{5.41}$$

$$Z_L(\omega_1) \simeq Z_L(\omega_2) \tag{5.42}$$

Using (5.40)-(5.42) and

$$V = \sqrt{2.P_{in} \cdot Z_o} \tag{5.43}$$

where P_{in} is the input power per tone, the IM_3 performance of the MESFET amplifier was evaluated; this was done as a function of the frequency and input power level of a two-tone test signal for different gate-bias voltages of the transistor. The intercept point P_I was obtained by extrapolating the small-signal fundamental and IM_3 product output, into the large-signal region.

5.4 Theoretical And Experimental Results:

The experimental results were obtained by applying a two-tone signal at the input of the amplifier. The two tones were obtained by using a Va-244A J-band Klystron source and a Varactor-tuned Gunn oscillator (Varian VSC 901984). The frequency of operation of both signal sources is dependent on ambient temperatures and the line voltages. For example the frequency stability of the Klystron is specified to be ±360 KHz/°C at 6 GHz due to temperature variations alone. Changes in line voltages of ±10% cause a further instability of ± 1.2 MHz. For the two-tone test it is essential that the frequency difference between the two sources remains constant. Therefore the two sources were operated in a master-slave relationship, with the Klystron source acting as the master source and the the Gunn oscillator tracking its frequency as a slave source. The locking of the two microwave sources was obtained through a frequency-locked loop mechanism. The two sources are combined together using a magic tee as a power combiner. The combined signal from one of the arms of the magic tee is down-converted using a mixer diode and the difference signal is filtered out with a low pass filter. This difference signal is compared to an extremely stable 1 MHz quartz crystal oscillator (HP 105A). A dc voltage proportional to the frequency difference between two signals is obtained. This dc voltage is applied to the varactor diode of the Gunn oscillator for electronic tuning. The locking circuit automatically maintains the frequency difference between two sources equal to 1 MHz. The circuit arrangement for measurement of the intermodulation distortion performance of the GaAs FET amplifier is shown in Fig. 5.8.

The resulting IM_3 was measured using a spectrum

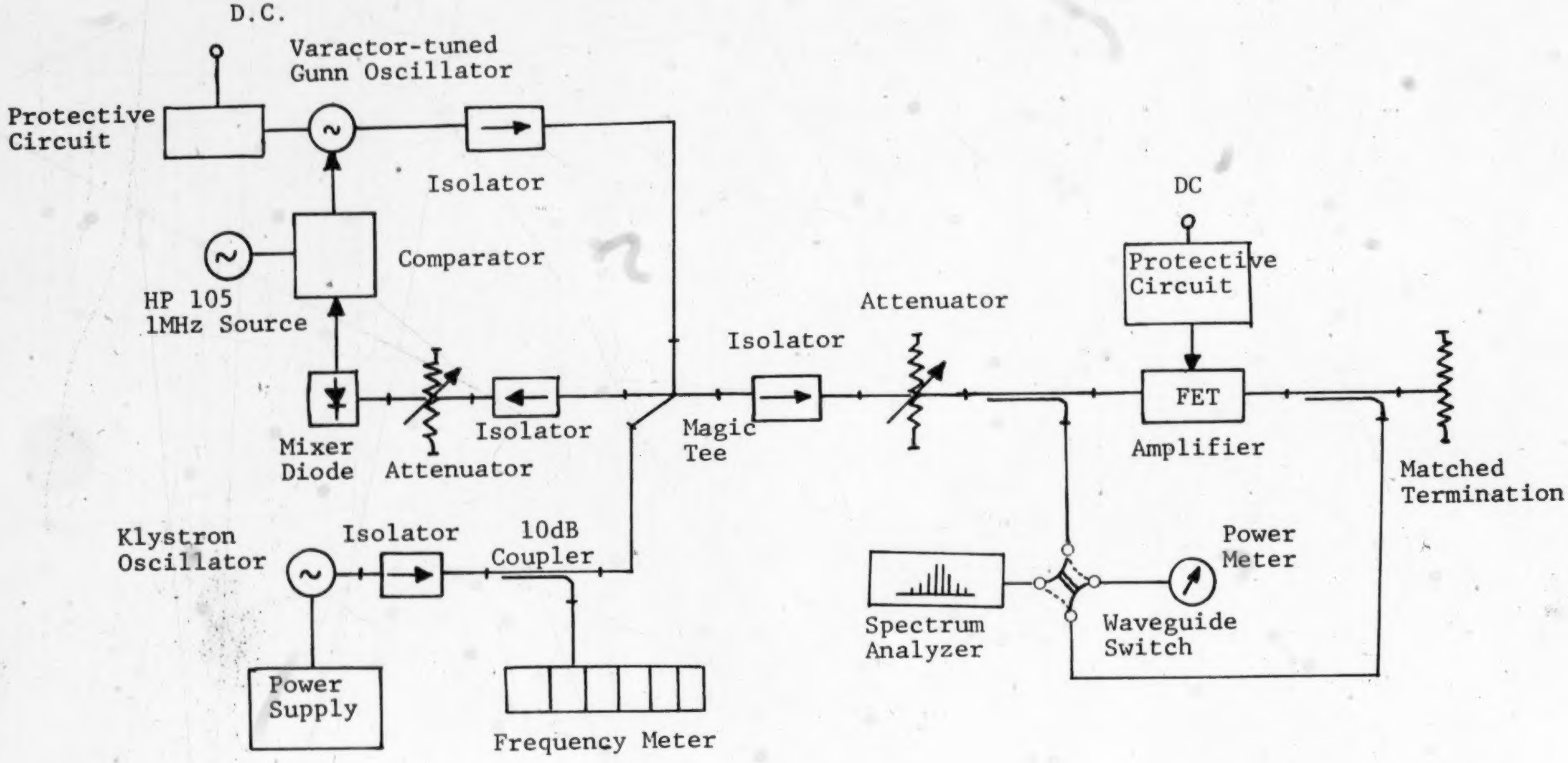
D.C.
Varactor-tuned Gunn Oscillator
Protective Circuit
Isolator
Comparator
HP 105 1MHz Source
Mixer Diode
Attenuator
Isolator
Magic Tee
Isolator
Attenuator
DC
Protective Circuit
FET
Amplifier
Matched Termination
Klystron Oscillator
Isolator
10dB Coupler
Power Supply
Frequency Meter
Spectrum Analyzer
Waveguide Switch
Power Meter

Fig. 5.8 The Circuit Arrangement for Measurement of the Intermodulation Distortion Performance of the GaAs FET Amplifier

analyzer. For the two tones at 6.000 GHz and 6.001GHz, the fundamental and the distortion product power output are plotted in Fig 5.9 as a function of input power level per tone. The measured results are seen to be in good agreement with the predicted values. As the power level is increased the measured IM_3 deviates from the predicted results, because 1)contributions from higher-order distortion products increase 2)the dc component of the output changes the bias conditions on the device and 3)the quasi-linear approximation does not remain valid at higher input power-levels. The frequency dependence of IM_3 for various input power levels is plotted in Fig 5.10. For a small-signal input of -10 dBm, the agreement between measured and predicted IM_3 is within 3-dB over an amplifier bandwidth of 400 MHz. The distortion is observed to be a maximum at the frequency where $|S_{22}|$ for the overall amplifier is minimum; that is, in the frequency region, where the device sees an impedance match at its output. This observation is consistent with the results of a recent study of the intermodulation distortion in a GaAs FET, by Tucker[64]. It may be concluded here, therefore, that an improved distortion performance can be obtained from a GaAs FET by detuning the device from conjugate match region at its output. Such detuning results in improvement of the distortion at the cost of the amplifier gain. The dependence of the intermodulation distortion on the gate-bias voltage is shown in Fig. 5.11. The IM_3 is observed to decrease by

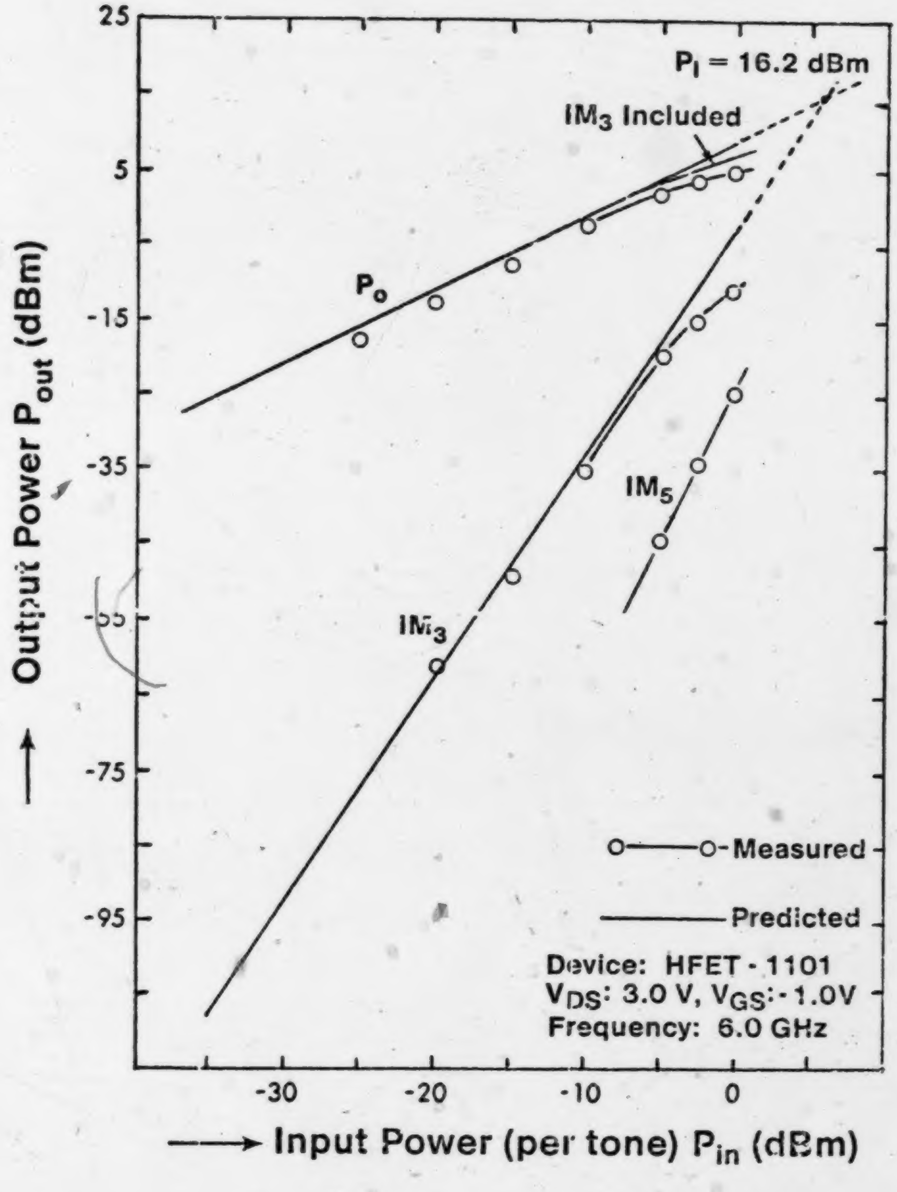

Fig. 5.9 Dependence of Fundamental and Intermodulation Product Output on Input Power Level; (Two-Equal Amplitude Tones: f_1 = 6.000 GHz, f_2 = 6.001 GHz)

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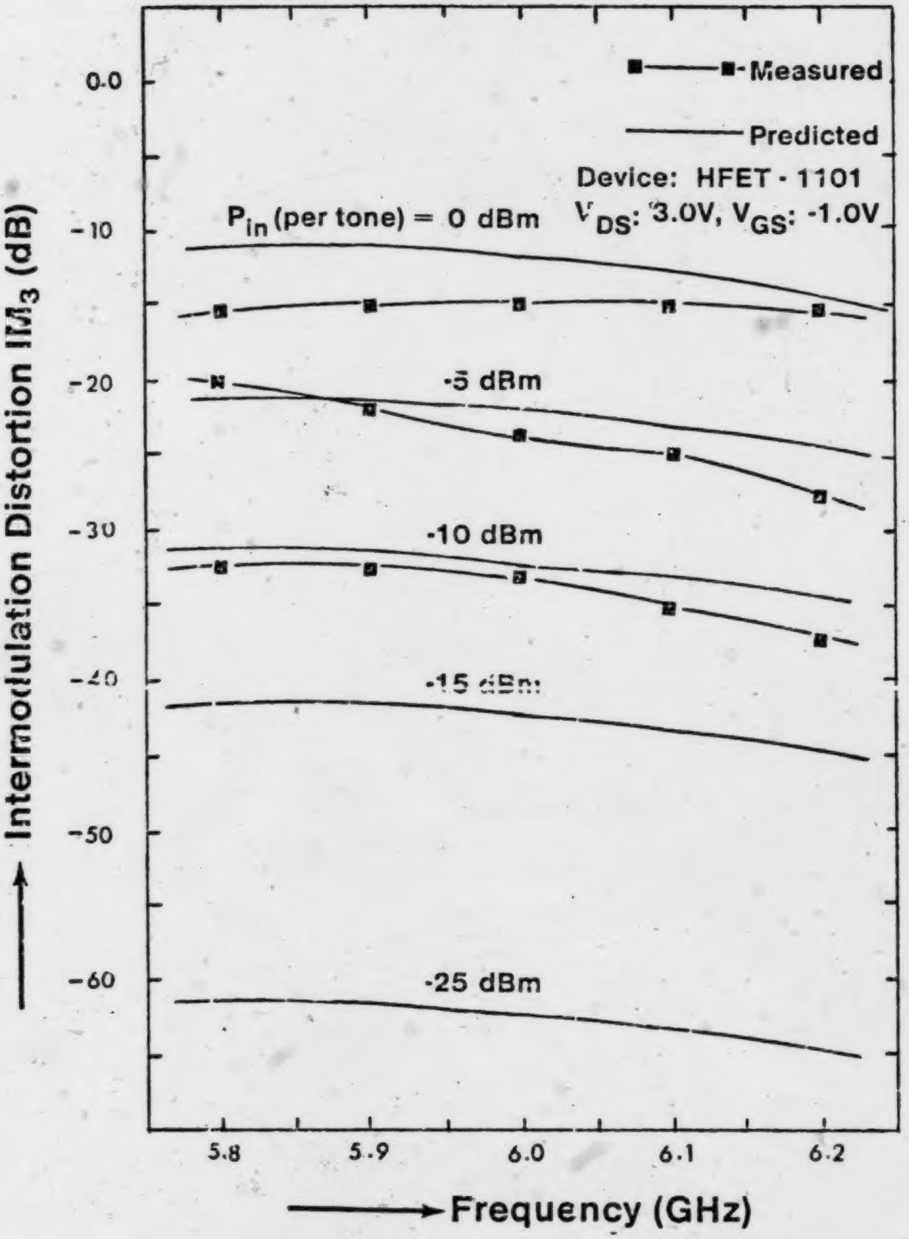

Fig. 5.10 Dependence of the Amplifier's IM_3 on the Frequency of the Two-Tone Signal, for Several Input Power Levels

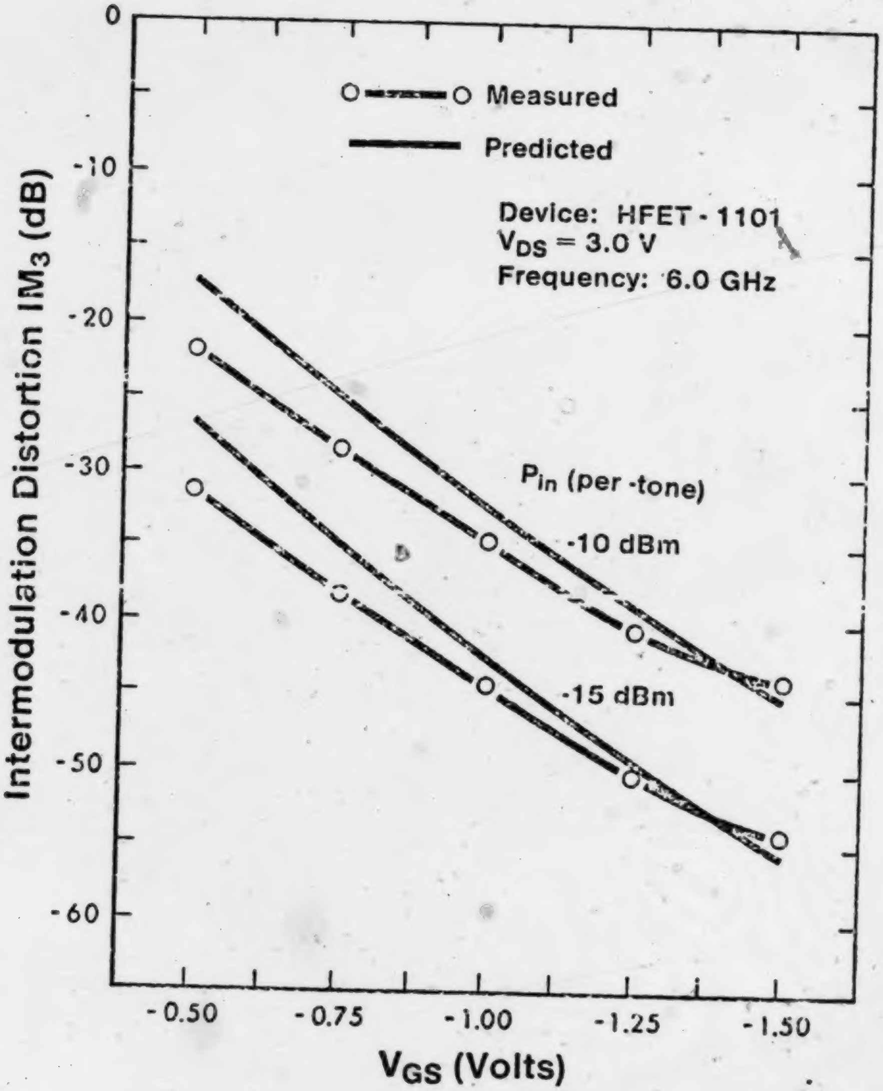

Fig. 5.11 Dependence of the Amplifier's IM_3 on the Gate-Bias Voltage for Several Input Power Levels

approximately 6-dB for -0.25V change in the gate-bias, in the current-saturation region of the device operation. Near the pinch-off region the IM_3 increases rapidly, as should be expected. The mechanism of generation of the intermodulation distortion in a GaAs FET amplifier involves the generation of distortion currents within the device because of device nonlinearities and their subsequent amplification because of gain mechanism of the device. The nonlinear coefficient associated with g_m increases with increasing negative gate-bias, but the coefficients associated with C_{gs} and C_{dg} are reduced in magnitude. The gain of the device decreases for increasing negative gate-bias. This interaction of the device nonlinearities and its gain result in decrease of distortion till a point of inflection is reached after which the distortion increases. For a given source and load impedance, the intercept point depends on the frequency of the two-tone signal and the transistor bias conditions. The intercept point increases with increasing negative gate-bias. This observation is consistent with the experimental observation of Liechti and Tillman[65]. For V_{GS} =-1.0V the experimental value of the intercept point of +16.5 dBm compares well with the predicted value of +16.2 dBm.

5.5 Improvement of Intermodulation Distortion

In communication system applications, microwave amplifiers need to be operated near the limit of their maximum power output. The intermodulation distortion at such power levels also increases. Traditionally, the input power levels are backed-off by 6 to 10 dB in order to meet acceptable performance standards. The 'back-off' represents a corresponding reduction in efficiency since dc operating conditions must be maintained at the original levels. Alternately, the intermodulation distortion may be reduced by using external adaptive techniques. Feedforward [70],[71] and predistortion [72] have been suggested as means of improving distortion performance of microwave amplifiers. Feedforward network basically consists of two loops; an auxiliary loop in which a sample output from the main amplifier is compared with the input signal and an error signal is generated. The error signal only consists of undesired components. In a second correction loop, the error signal is amplified and combined with the the output signal from the amplifier. The gain and phase in the correction loop are adjusted such that the undesired components of the output signal are nulled. Predistortion involves passing the multiple-carrier signal through a network with inverse nonlinear amplitude characteristics. The transformation of the predistorted signal through the amplifier results in reproduction of the original signal. The derivation of the transfer function for the equalization circuit and its practical realization remains a problem of considerable difficulty. Feedforward and predistortion techniques have advantages over the conventional back-off approach in that the amplifier can be operated in the region of increased dc to RF conversion efficiency. They also result in increased system complexity, increased cost and power consumption. In this section, a gate-bias compensation technique is described that results in improved distortion performance of the amplifier for increasing input microwave power-levels[73]. A similar technique has been used to improve the distortion in a 13-GHz IMPATT amplifier[74].

For low-level input signals it is desirable that the FET amplifier should be operated at larger drain-currents to achieve higher gain. Such an operating point results in a reduced bandwidth, as seen in Figure 5.7, and increased noise figure[75]. It has been pointed out in previous section that the intermodulation distortion performance of the amplifier is also degraded. The third-order intermodulation distortion small-signal gain results obtained for the GaAs FET are shown in Fig. 5.12. The small-signal gain of the amplifier, for gate-to-source voltage V_{GS} =-0.5 V and drain-to-source voltage V_{DS} =3.0V, is 11.2 dB and it reduces as the gate voltage is made more negative. The intermodulation distortion also reduces as the gate-bias is made more negative (reduced drain current). A minimum of IM_3 is observed for V_{GS} =-1.52 V. Beyond this gate-bias, the IM_3 product increases rapidly because of device operation near the pinch-off voltage. The intermodulation product was observed to depend on the drain-bias also; it increases for reduced drain-bias voltage

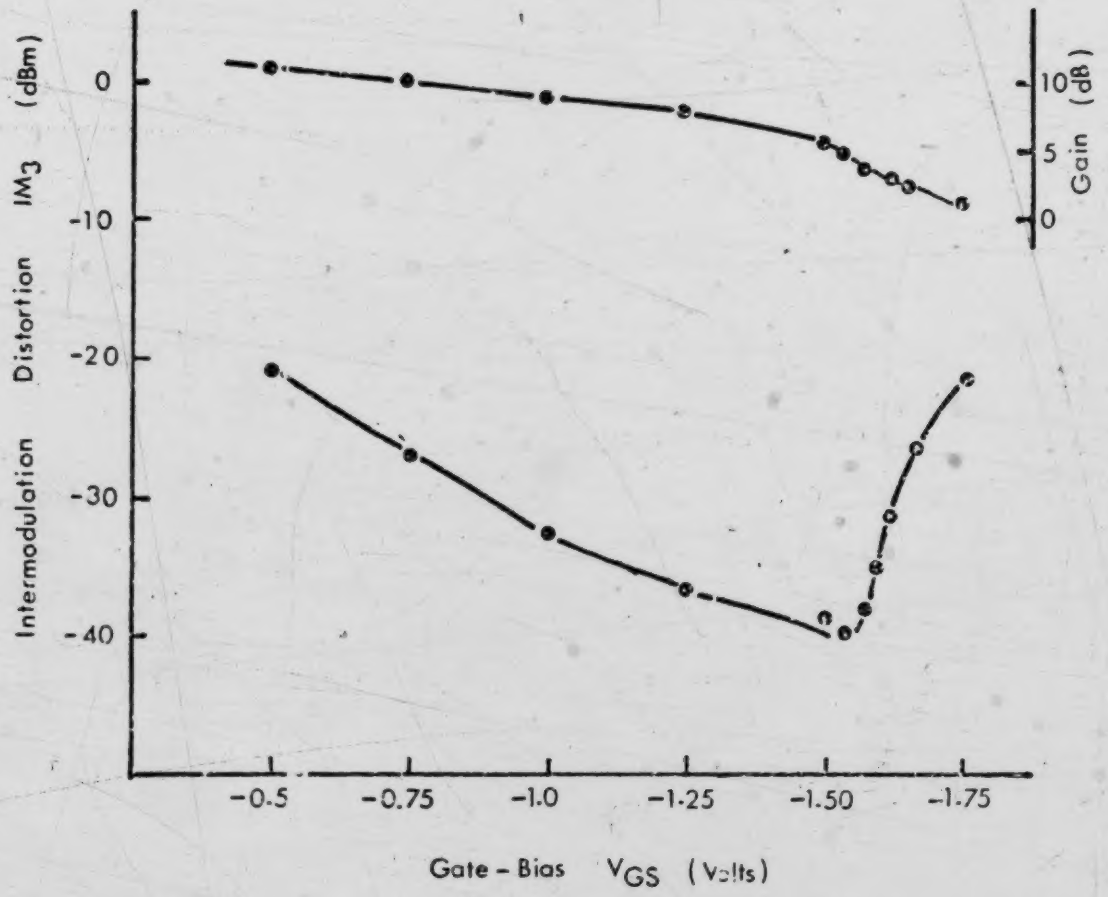

Fig. 5.12 Small-Signal Gain and Third-Order Intermodulation Distortion (IM_3) as a Function of the Gate-Bias V_{GS}

and decreases as the drain-bias is increased.

Fig. 5.13 depicts a schematic diagram of the gate-bias compensation technique for reduction of the distortion. The detected output from the diode detector is amplified and added in a negative sense to the gate-bias voltage, so that when the input power increases the gate-bias becomes more negative. This results in a decrease of the amplifier gain as well as of the IM_3 product. The IM_3 reduces more rapidly than the gain, resulting in a net improvement in the distortion product.

The signal spectrum at the output of the uncompensated amplifier, for a two-tone input signal is shown in Fig. 5.14(a). For 0 dBm output per tone, the IM_3 product is -27.5 dBm. When the input signal is increased by 2 dB ,the intermodulation product increases to -22.5 dBm. With the gate-compensation applied, the gain of the amplifier in the compensation loop can be adjusted so that the output power at the fundamental frequency tones is 0 dBm. The IM_3 product is now observed to be -37.5 dBm which is a 10 dB improvement. The resulting output signal spectrum is shown in Fig. 5.14(b).

For small signals the compensation does not noticeably affect the performance of the amplifier. At larger signal levels (P_{out} approx. -10 dBm) the gate-bias is affected by the input signal and the gain decreases with increasing input power. This tends to produce a constant output power, which may be advantageous in some applications. For large

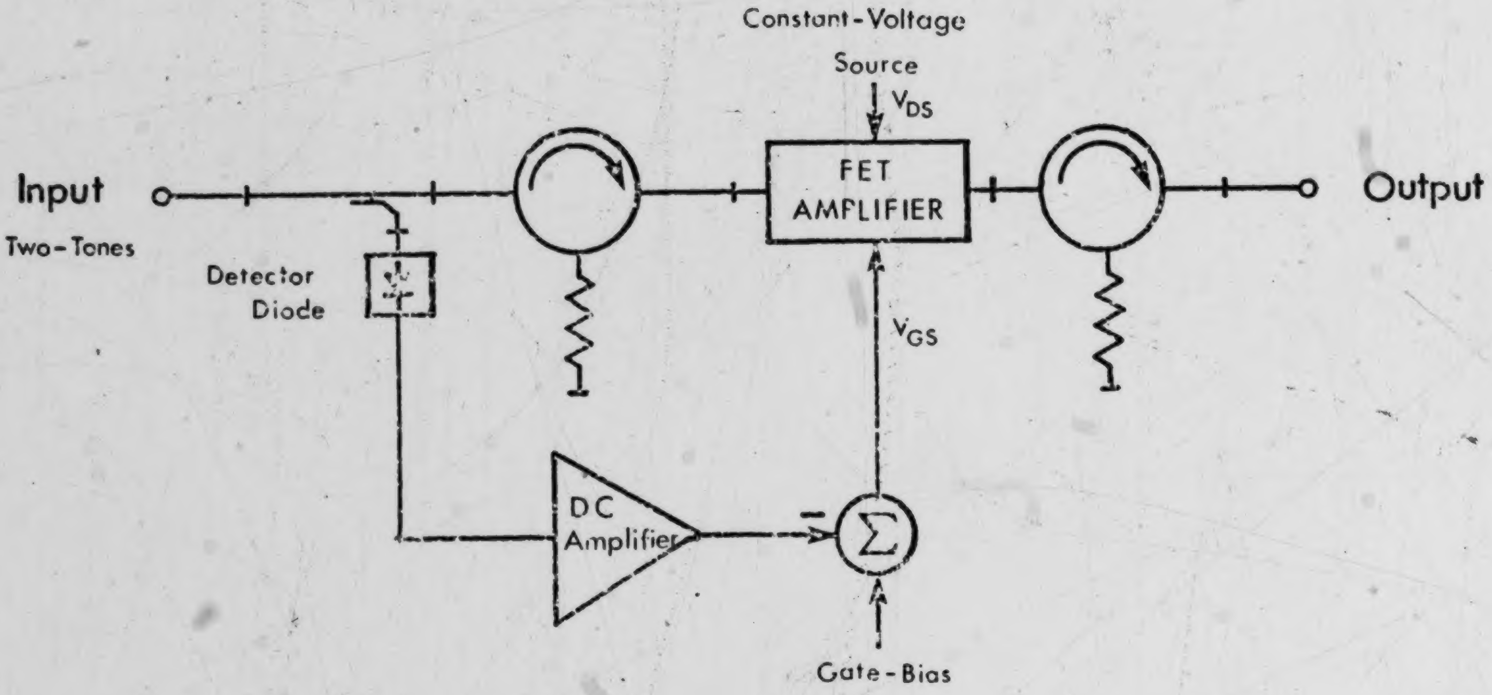
Input
Two-Tones
Detector
Diode
Constant-Voltage
Source
V_{DS}
FET
AMPLIFIER
V_{GS}
DC
Amplifier
−
Σ
Gate-Bias
Output

Fig. 5.13 A Schematic Diagram of the Gate-Bias Compensation Technique for Improvement of Distortion

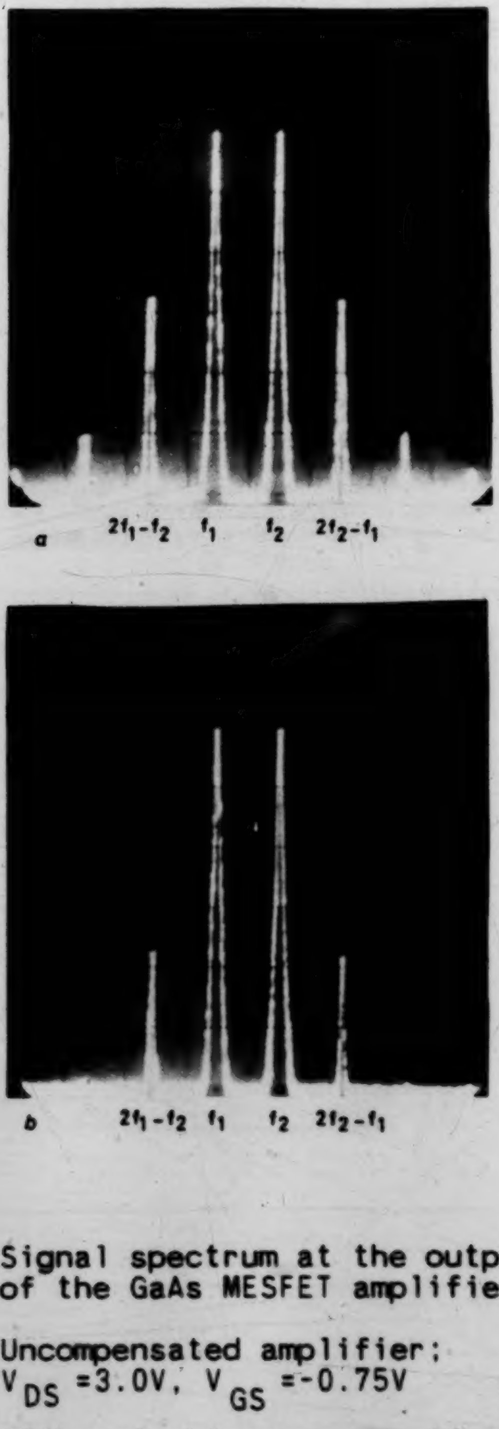

Fig. 5.14 Signal spectrum at the output of the GaAs MESFET amplifier.

a) Uncompensated amplifier; V_{DS} =3.0V, V_{GS} =-0.75V

b) With gate-bias compensation

input signals the gate-bias approaches the pinch-off voltage, causing a reduction in gain and an increase in intermodulation distortion. This is a limiting factor for the range over which the compensation is effective. Furthermore, the second amplifier in the compensation loop adds some noise to the FET amplifier gate-circuit, thus degrading the overall noise performance.

5.6 Computation of Cross modulation Distortion

Cross modulation distortion occurs when a number of amplitude modulated signals are applied to the amplifier input. Because of the device nonlinearities, a transfer of modulation takes place from one carrier to another. For analysis and measurement of cross modulation distortion, two signals of equal amplitude at frequencies ω_1 and ω_2 one modulated and another initially unmodulated, are considered as input signals.

$$V_{in}(t) = V(1 + b_1 \cos\omega_m t)\cos\omega_1 t + V\cos\omega_2 t \qquad (5.44)$$

b_1 is the modulation index , ω_m is the modulation frequency and V is the signal amplitude.

Equation (5.44) can be rewritten in the following form.

$$V_{in}(t) = \frac{V}{2}\ [\exp(j\omega_1 t) + \frac{b_1}{2}\exp[j(\omega_1+\omega_m)t] + \frac{b_1}{2}\exp[j(\omega_1-\omega_m)t]$$

$$+ \exp(j\omega_2 t) + \text{C.C.}] \qquad (5.45)$$

where CC represents the complex conjugate terms.

The second-order and all even-order nonlinearities do not contribute towards the cross modulation term. For small distortion, the third-order term will be the major contributor to the distortion. The steady state response at the amplifier output, in terms of Volterra transfer functions is given by

$$y_{\omega_2+\omega_m} = \frac{1}{8}\,\frac{b_1}{2}\,[V_{o_3}(j\omega_1,-j(\omega_1+\omega_m),j\omega_2)\exp(j\omega_2 t).$$

$$\exp(-j\omega_1+\omega_m)t)\exp(j\omega_2 t)$$

$$+\;V_{o_3}(-j\omega_1,j(\omega_1+\omega_m),j\omega_2)\exp(-j\omega_1 t).$$

$$\exp(j(\omega_1+\omega_m)t).\exp(j\omega_2 t)$$

$$+\;\ldots\ldots\ldots\;+\;C.C.] \qquad (5.46)$$

There are a total of 12 terms plus their complex conjugates. Taking only the real parts, and for $\omega_m << \omega_1$ (5.46) may be written in the following form

$$y_{\omega_2+\omega_m} = \frac{1}{2}\,\frac{b_1}{2}\;.\;3V_{o_3}(j\omega_1,-j\omega_1,j\omega_2).\exp(j(\omega_2+\omega_m)t)$$

$$+\;C.C. \qquad (5.47)$$

$$= \frac{3}{2}\,|V_{o_3}(j\omega_1,-j\omega_1,j\omega_2)|\cos[(\omega_2+\omega_m)t + \beta_2] \qquad (5.48)$$

where the argument

$$\beta_2 = \angle \underline{V_{o_3}(j\omega_1,-j\omega_1,j\omega_2)} \tag{5.49}$$

The total output, including the fundamental frequency component, will be given by

$$y_o(t) = |V_{o_1}(j\omega_2)|\cos(\omega_2 t + \beta_1)$$

$$+\ 3b_1|V_{o_3}(j\omega_1,-j\omega_1,j\omega_2)|\cos(\omega_2 t+\beta_2)\cos\omega_m(t) \tag{5.50}$$

$$= |V_{o_1}(j\omega_2)|[\cos(\omega_2 t+\beta_1) + b_x\cos(\omega_2 t+\beta_2)\cos\omega_m t] \tag{5.51}$$

where

$$b_x = 3b_1 \frac{|V_{o_3}(j\omega_1,-j\omega_1,j\omega_2)|}{|V_{o_1}(j\omega_2)|} \tag{5.52}$$

$$\beta_1 = \angle \underline{V_{o_1}(j\omega_2)} \tag{5.53}$$

$$\beta_2 = \angle \underline{V_{o_3}(j\omega_1,-j\omega_1,j\omega_2)} \tag{5.54}$$

The cross modulation factor is defined as

$$(CM)_F = \frac{b_x}{b_1} = \frac{3|V_{o_3}(j\omega_1,-j\omega_1,j\omega_2)|}{|V_{o_1}(j\omega_2)|} \tag{5.55}$$

Equation (5.50) may be rewritten as

$$y_o(t) = |V_{o_1}(j\omega_2)|(1 + b_x \cos\phi \cos\omega_m t)\cos(\omega_2 t + \beta_1 +$$

$$b_x \sin\phi \cos\omega_m t) \tag{5.56}$$

Both amplitude and phase modulation will occur. Amplitude cross modulation at high freuencies is defined as the ratio of the fractional transferred amplitude modulation to the original fractional amplitude modulation.

$$(CM)_A = \frac{b_x \cos\phi}{b_1} = (CM)_F \cos\phi \tag{5.57}$$

The phase cross modulation factor (CM) is defined as the ratio of the transferred phase modulation to the original fractional amplitude modulation.

$$(CM)_\phi = \frac{b_x \sin\phi}{b_1} = (CM)_F \sin\phi \tag{5.58}$$

The computed values of cross modulation as a function of the signal frequency and input power levels are shown in figures 5.15(a) and 5.15(b). The frequency dependence shows that the magnitudes of $(CM)_A$ and $(CM)_\phi$ are strongly dependent on frequency, and are equal at a frequency of approximately 6 GHz. The dependence of the cross modulation distortion on input power level is plotted for a frequency of 5.8 GHz, where AM to PM conversion factor is approximately 5.5 dB higher than AM to AM conversion factor. At an input power level of -10 dBm the AM to PM conversion factor is computed to be -20 dB and AM to AM conversion factor is -25.5 dB.

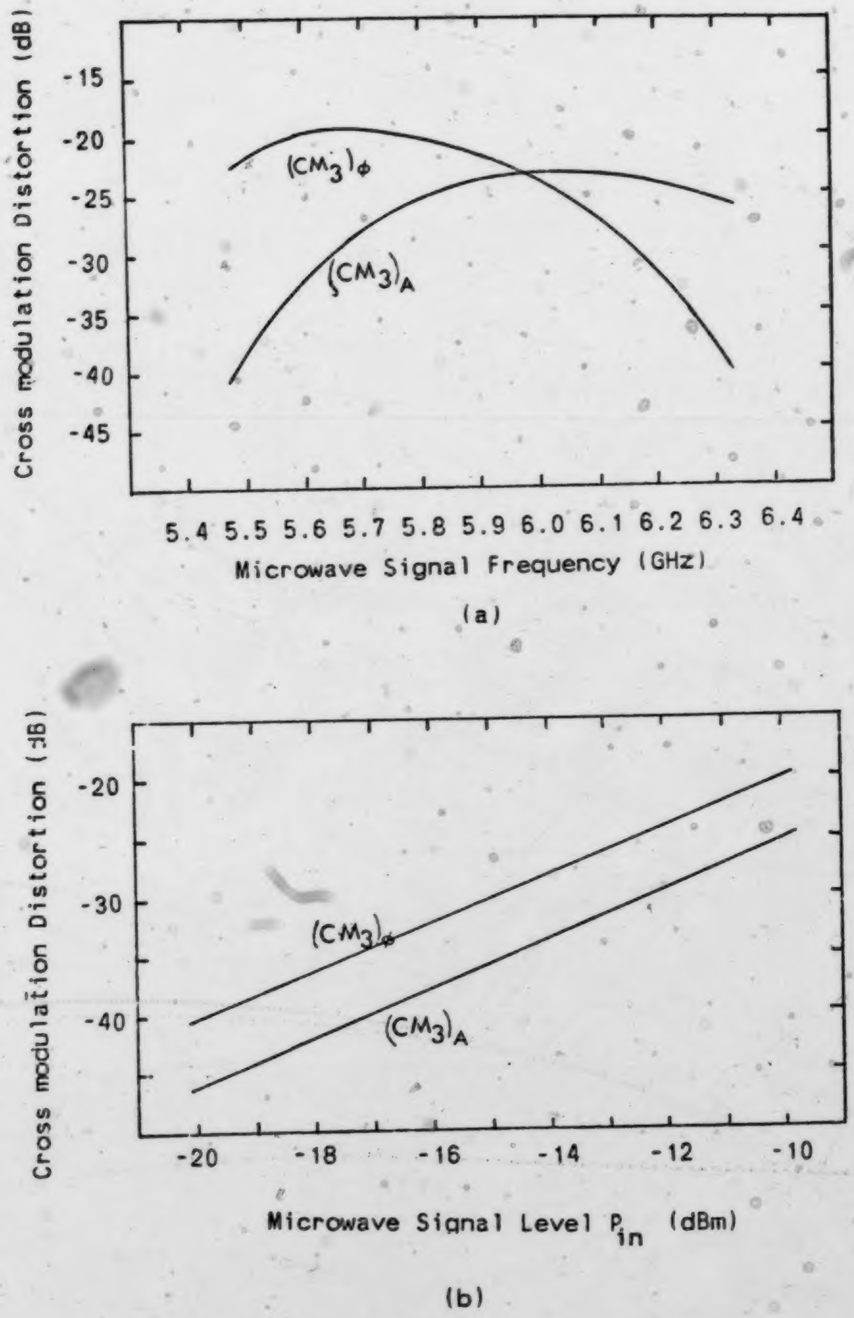

Fig. 5.15 Computed Cross Modulation Distortion Factor for a GaAs FET Amplifier

(a) As a Function of Signal Frequency

(b) As a Function of Input Power Level

5.7 Gain Compression in GaAs FET Amplifiers

For small-signal, single frequency inputs, the amplifier output increases linearly with the input signal. As the signal strength is increased the amplifier output tends to saturate and the gain of the amplifier decreases. The gain compression (or expansion) is caused by the odd-order nonlinearities within the device. Such nonlinearities contribute terms towards the fundamental frequency component of the amplifier output. Volterra-series analysis techniques can be used to investigate the behaviour of the amplifier response as the input power levels are increased beyond the small-signal linear gain response region. A single-frequency input signal with frequency and amplitude V may be represented as

$$V_i(t) = V \cos\omega_1 t \tag{5.59}$$

The output signal at frequency may be represented as

$$\begin{aligned} V_o(\omega_1) = {} & |V_{o_1}(j\omega_1)| \cos(\omega_1 t + \angle V_{o_1}(j\omega_1)) \\ & + \frac{3}{4} |V_{o_3}(j\omega_1, j\omega_1, -j\omega_1)| \cos(\omega_1 t + \angle V_{o_3}(j\omega_1, j\omega_1, -j\omega_1) \\ & + \text{higher-order terms} + \ldots. \end{aligned} \tag{5.60}$$

The third-order nonlinearity makes the largest contribution to the gain compression. Therefore, the departure of the amplifier gain response from linearity can be examined by ignoring the higher-order terms in (5.60). The total magnitude and phase at the amplifier output can be obtained by the vector sum of the two components. The magnitude of $V_o(j\omega_1)$ of the output response can be expressed in the following form

$$|V_o(j\omega_1)| = \sqrt{|V_{o_1}(j\omega_1)|^2 + |V_{o_3}(j\omega_1,j\omega_1,-j\omega_1)|^2 + |V_{o_1}(j\omega_1)|\,|V_{o_3}(j\omega_1,j\omega_1,-j\omega_1)|\cdot\cos(\gamma_3 - \gamma_1)} \qquad (5.61)$$

and the phase deviation as

$$\Delta\phi = \mathrm{Tan}^{-1}\left[\frac{|V_{o_3}(j\omega_1,j\omega_1,-j\omega_1)|\sin(\gamma_3-\gamma_1)}{|V_{o_1}(j\omega_1)|+|V_{o_3}(j\omega_1,j\omega_1,-j\omega_1)|\cos(\gamma_3-\gamma_1)}\right] \qquad (5.62)$$

where

$$\gamma_3 = \angle V_{o_3}(j\omega_1,j\omega_1,-j\omega_1) \qquad (5.63)$$

$$\gamma_1 = \angle V_{o_1}(j\omega_1) \qquad (5.64)$$

It should be pointed out here that the arguments of the first order and third-order contributing components are frequency dependent and a difference of these arguments appears in the expressions for total magnitude and phase. This difference in phase angles determines the gain compression or expansion. The gain in dB was computed from

$$G_o(\mathrm{dB}) = 20\,\log_{10}\left|\frac{V_o(\omega_1)}{V}\right| \qquad (5.65)$$

The gain of the amplifier in the large signal region was computed at 6 GHz as a function of input power level. The comparison in measured and computed gain is shown in Figure 5.16. It is observed that the input level at which 1-dB gain compression occurs is dependent on the transistor gate-bias voltage. Gain compression occurs at relatively smaller input power levels for less negative gate-bias voltages (larger gain). This is to be expected because of limited output capabilities of the device. The agreement between measured and computed gain is observed to be good for gate-bias voltages of -1.5V, -1.25V and -1.0V. For gate-bias voltage of -0.5 and -0.75V the agreement deteriorates, because of larger device gain and large nonlinearities. The phase deviation due to device nonlinearities is a function of frequency and input power-levels. The computed phase deviation as a function of input power levels at various frequencies is shown in Figure 5.17. The change in phase is observed to increase as the input power level is increased. This causes AM to PM conversion when an amplitude modulated signal is applied at the amplifier input. It is quite obvious from these results that the AM to PM conversion is frequency and power level dependent. At input levels of -10 dBm the conversion factor is observed to be 0.23 degree/dB. The results for phase deviation were not experimentally varified because a suitable measurement arrangement was not available.

The AM to PM conversion in a GaAs FET amplifier is

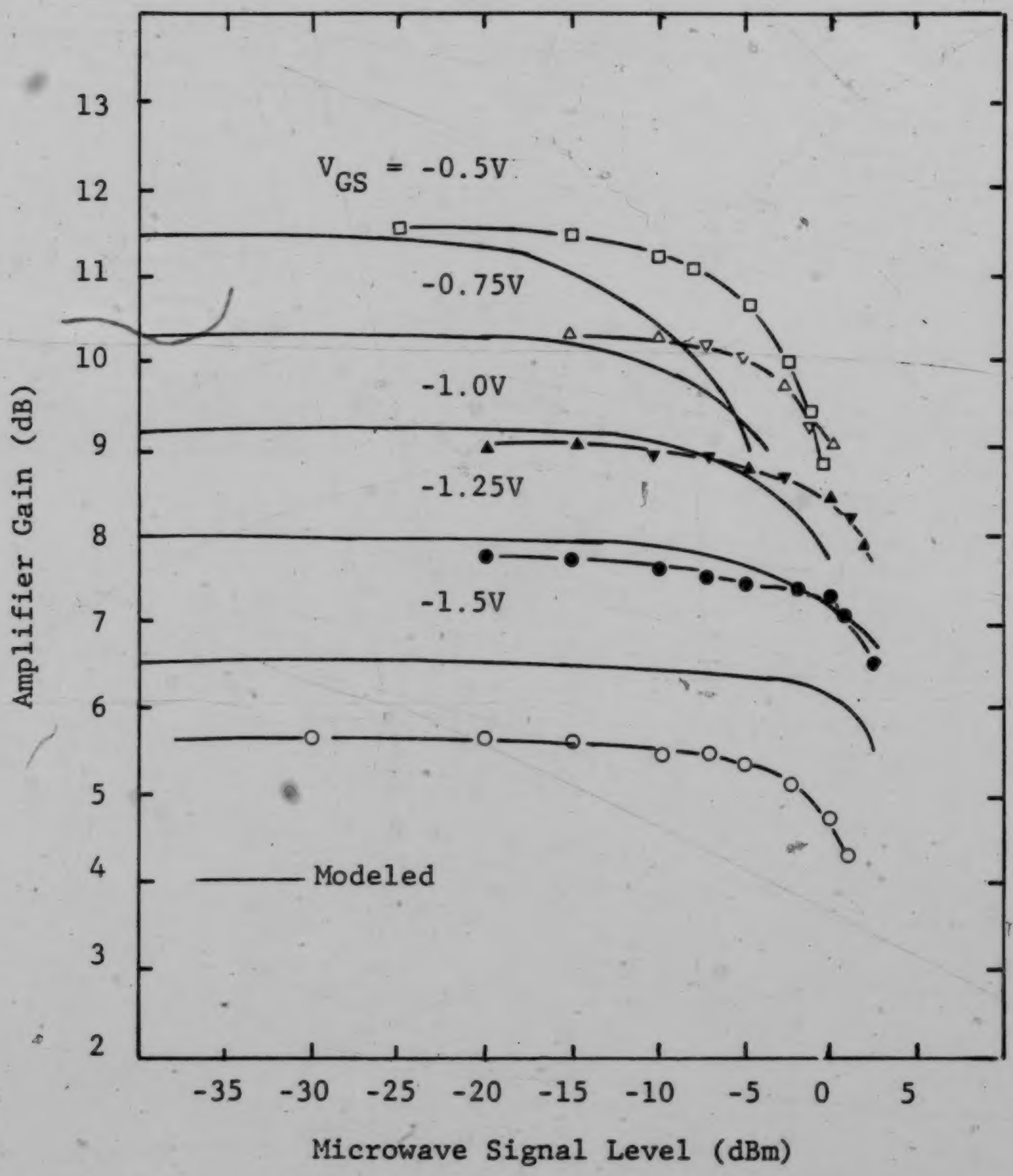

Fig. 5.16 Gain Compression in the GaAs FET Amplifier; Device HFET-1101, V_{DS} = 3.0V, Frequency = 6.0 GHz

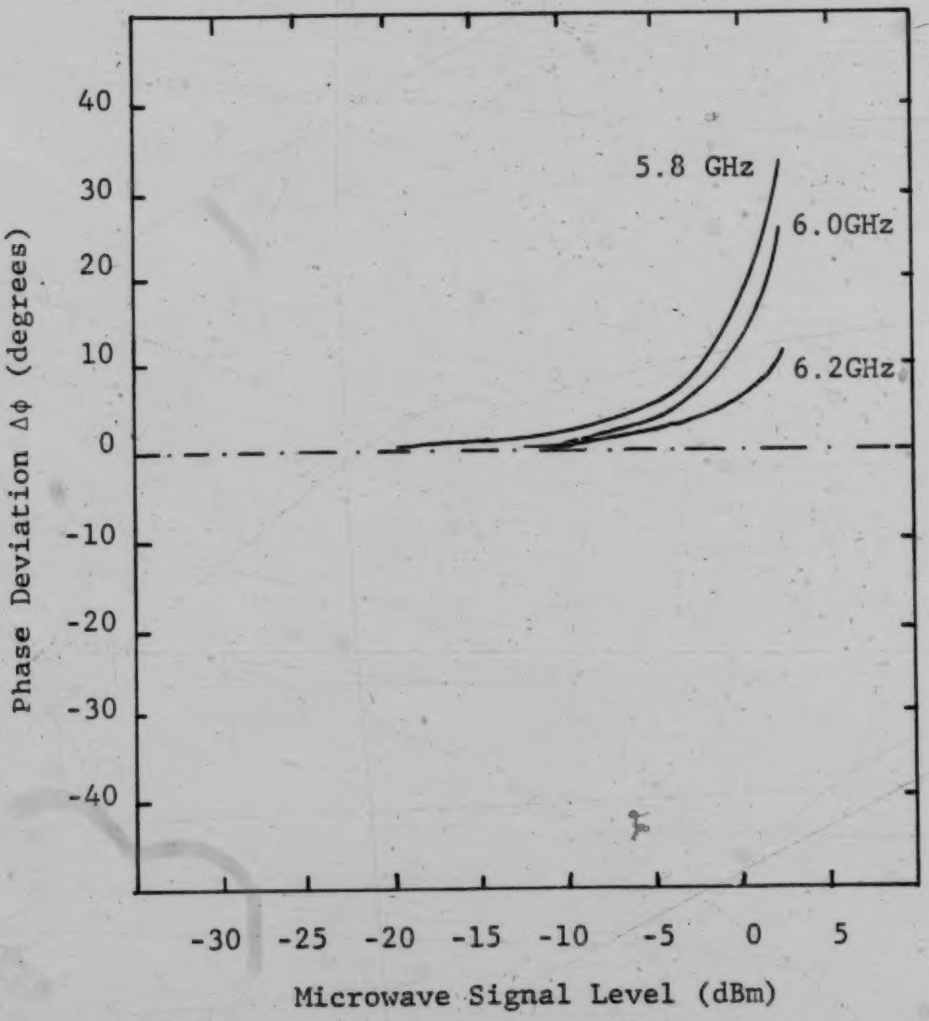

Fig. 5.17 Phase Deviation in the GaAs FET Amplifier as a Function of Input Power-Level; Device HFET-1101, V_{DS} = 3.0V, V_{GS} = -1.0V

observed to be less as compared to other solid-state devices such as IMPATT amplifiers. The third-order intercept point is observed to be much higher as compared to that in IMPATT amplifiers.

The Volterra-series expansion has been found adequate for predicting the intermodulation distortion, the gain compression and phase deviation in a GaAs FET amplifier, for small input signals. These results have been obtained for a low-power device. As has been pointed out in Section 5.3.4, the nonlinear response of high power GaAs FET's is not well-behaved. Therefore, the concept of intercept point, 1-dB compression point,and cross modulation factors cannot be used for high power devices.

CHAPTER VI

UP-CONVERSION IN A SINGLE-GATE GaAs FET AMPLIFIER

In this chapter, a method is described for achieving up-conversion in a single-gate MESFET amplifier. A mathematical model is proposed for analysis of the up-conversion characteristics of the amplifier. The proposed model is basically an extension of the Volterra-series model developed in Chapter V. The model takes into account the device nonlinearities and their interaction with the impedances seen by the device at the various frequency components which are present at the input and output of the amplifier. The theoretically predicted results are compared with the experimental observations.

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6.1 Introduction

Frequency converters commonly used in microwave heterodyne communication systems use nonlinear two-terminal devices such as Schottky-barrier diodes. Active mixers using GaAs FETs have been demonstrated recently [76]-[82], which offer advantages of larger bandwidth, low noise, larger dynamic range and the possibility of conversion gain. The dynamic range of GaAs FETs is about 10 dB greater than that of Schottky-barrier mixer diodes, and their power handling capacity is some 15 dB greater[76]. These properties are particularly attractive for applications at frequencies towards the higher end of the microwave range and millimeter wave frequency range, where relatively few devices are available that can offer conversion gain. Previous studies of the frequency mixing mechanism of FETs have been limited to their application in down-converters, with the output intermediate frequency (IF) signal being the difference between two applied input signals.

This chapter will focus on another application of mixers, namely microwave up-conversion. Dual-gate microwave field effect transistors have been used for achieving upconversion; gains up to 14 dB have been reported [79]. Dual-gate devices often require an extensive design procedure because of the measurement difficulties posed by three-port S-parameters, as well as the design of three independent matching circuits. The up-converter described here uses a single-gate MESFET amplifier. A model is proposed for determining the theoretical up-conversion characteristics. These characteristics are studied as a function of parameters extrinsic to the device, such as gate-bias, IF signal level, and microwave frequency. Experimental results have been obtained for a GaAs FET device, and comparison is made with the theoretically predicted results.

6.2 Experimental Set Up

A schematic diagram for obtaining up-conversion using a MESFET is shown in Figure 6.1. The microwave signal is

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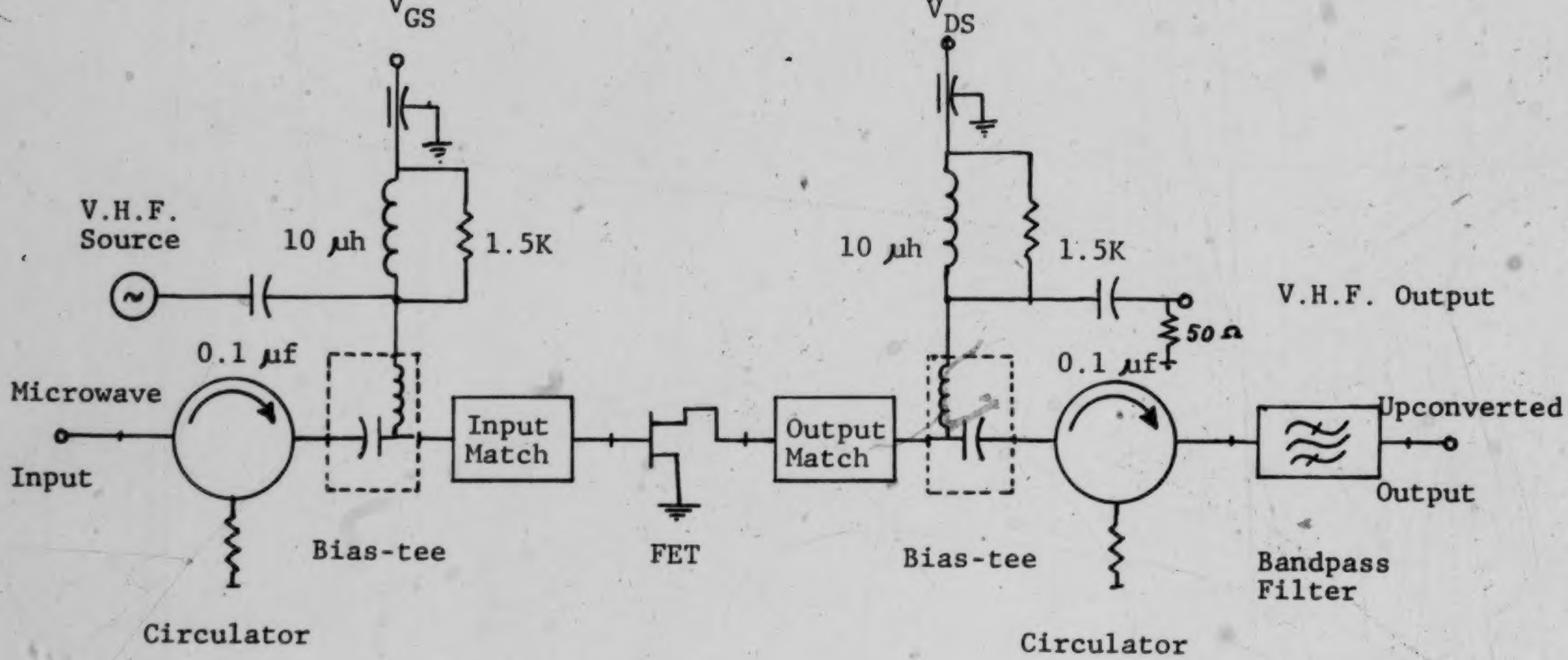

V_{GS}
V_{DS}
V.H.F. Source
10 µh
1.5K
10 µh
1.5K
V.H.F. Output
50 Ω
0.1 µf
0.1 µf
Microwave Input
Input Match
Output Match
Upconverted Output
Bias-tee
FET
Bias-tee
Bandpass Filter
Circulator
Circulator

Fig. 6.1 A Schematic Diagram for Obtaining Up-Conversion Using a MESFET

applied through a circulator at the input of the amplifier and the IF signal is impressed on the gate-bias circuit. A 10 μh RF choke and 1.5 K ohm resistances are used for isolating the dc power supply from the IF signal. A similar arrangement is used at the drain circuit of the MESFET. Because of the GaAs FET nonlinearities, side-bands are generated at sum and difference frequencies. An appropriate side-band can be filtered out using suitable bandpass filters.

Experimental results were obtained for a MESFET amplifier using an HP HFET-1101 device. No filters were used in the output circuit of this amplifier because of the unavailability of a suitable narrow-band filter. Use of such a filter should cause only a few dB of insertion loss and will not affect the essential characteristics of the up-converter. The circulator in the output circuit of the amplifier prevents any signals from being reflected back to the device. The microwave input signal level was kept at -5 dBm because the GaAs FET used is a low-power device and the gain of the amplifier saturates rapidly beyond this level.

6.3 Nonlinear Up-converter Model

For purposes of analysis, the problem of up-conversion consists of analyzing the interaction between two (or more) frequencies for a nonlinear device embedded in a microwave circuit. The nonlinearities of the device are assumed to be time-invariant and the associated microwave circuit has memory because of the reactive effects of the device parasitics and the equivalent circuit reactances. The input signal consists of two inputs which are essentially the sum of two sinusoidal waveforms. The microwave output at the sideband (up-converted) frequency depends upon the local oscillator (LO) power, the IF power, the device dc biasing and the embedding impedances presented to the device at all the component and harmonic frequencies of the input signals. Harmonic frequencies of the input microwave signal fall outside the amplifier band and therefore do not contribute towards the up-converted output signal.

A model that includes the dominant device nonlinearities and their interaction with the embedding impedances presented to the GaAs MESFET is shown in Figure 6.2. The device model is the same as described in the previous chapter. Three nonlinearities are assumed to contribute mainly to the mixing process; these are the gate-to-source capacitance C_{gs}, the transconductance g_m and the drain-to-gate capacitance C_{dg}. An averaged value of output resistance R_o can be used [5], [7], [58], [77] for frequency conversion analysis. $Z(f_o)$, $Z(f_o - f_1)$,……… are the embedding impedances at the input and output of the amplifier at various frequency components. These impedances are not a set of disjoint terminations but the impedances presented to the device at various frequencies. $H(f_o)$, $H(f_o - f_1)$,……… are assumed to be ideal filters, that have no insertion loss and allow currents to flow through the

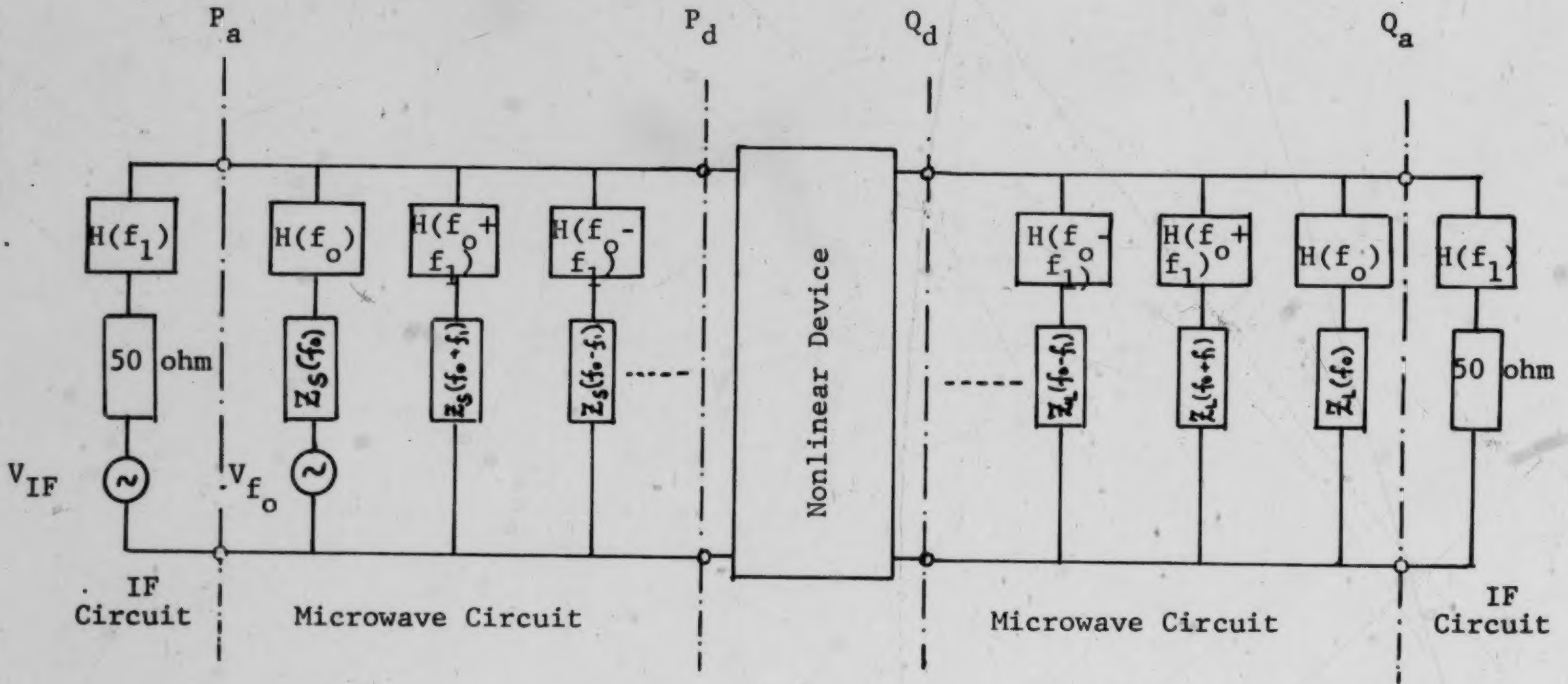

P_a
P_d
Q_d
Q_a
H(f_1)
50 ohm
V_IF
IF Circuit
V_f_o
H(f_o)
Z_s(f_o)
H(f_o+f_1)
Z_s(f_o+f_1)
H(f_o-f_1)
Z_s(f_o-f_1)
Microwave Circuit
Nonlinear Device
H(f_o-f_1)
Z_L(f_o-f_1)
H(f_o+f_1)
Z_L(f_o+f_1)
H(f_o)
Z_L(f_o)
H(f_1)
50 ohm
Microwave Circuit
IF Circuit

Fig. 6.2 A Model for Computation of Up-Conversion Characteristics of the GaAs FET Amplifier

(complex) circuit impedances at the respective frequencies only. The numerical values of these impedances were computed from the characterised microwave circuit surrounding the device as described in the previous chapter. The GaAs FET sees real impedances of 50 ohm at the IF signal frequency at both the input and the output of the device.

When a small-signal IF voltage is applied to the 'pumped' device, currents flow in the device at the frequencies ω_o, ω_1, $\omega_o \pm n\omega_1$, where ω_o is the LO or 'pump' frequency and ω_1 is the IF frequency and n=1,2,3,....... . Because of nonlinear elements in the GaAs FET both at the input and output of the device, the nonlinear currents will flow through the gate as well as through the drain circuit. Therefore, circuit impedances at the frequency components are included in both the input and the output circuit of the amplifier. Normally the first lower- or upper sideband is the largest in magnitude at the amplifier output and is filtered out. Therefore, in actual practice, it is necessary to compute the impedances presented by the microwave circuit at the lower- and upper sidebands only. Each nonlinear element in the device generates sideband components depending upon the magnitude of the nonlinearity and the signal strengths of the two interacting signals across the nonlinear element.

The second order coefficients were computed by interpolation of the device data for the nonlinear intrinsic elements C_{gs} , g_m , and C_{dg} . Their derivatives were computed at the operating gate-bias voltage.

6.4 Analysis of Up-conversion Characteristics

The up-conversion characteristics of the amplifier are analyzed using the Volterra-series approach described in section 5.3.3. For purposes of analysis, the impedances of the microwave circuit at the input and output of the device are separated into their real and imaginary parts, so that the same six nodes define the overall amplifier up-converter circuit. The numerical values of the terminating impedances at various frequencies are computed from the characterised and designed parameter values of the circuit surrounding the device. The device model remains the same as described in the previous chapter. The relationships between the input microwave power and the terminal voltages as described in equations (5.12) to (5.18) are used. Equations (5.19) to (5.24) define the overall amplifier up-converter model of Fig. 6.2. These equations can be rewritten in the following form

$$[A(j\omega)][V_{nm}(j\omega)] + [\text{Nonlinear Currents}] = I_{ni}(j\omega) \qquad (6.1)$$

$[A(j\omega)]$ is the six-by-six system matrix with complex coefficients and is described in Figure 5.6. The first-order kernels (linear potentials) were conveniently computed by ignoring the nonlinear currents, and using the matrix inversion

$$V_{n1}(j\omega) = [A(j\omega)]^{-1}[V_{1i}(j\omega)] \tag{6.2}$$

where

$$V_{1i}(j\omega) = \begin{bmatrix} \dfrac{2v_1^+}{R_e\{Z_S(\omega)\}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{6.3}$$

Equations (6.2) and (6.3) were solved numerically, at both the microwave pump frequency and the IF signal frequency. An IF frequency of 70 MHz was chosen for the analysis and measurement of the up-conversion characteristics. At 70 MHz, the numerical values of jX_S and jX_L are both zero and $Re\{Z_S(\omega)\}$ in (6.3) is 50 ohms. At the IF frequency some of the matrix elements become very small and the matrix tends to become ill-conditioned. Extended precision arithmetic and a high accuracy solution were therefore used. $[V_{n1}(j\omega)]$ ($n=1$ to 6 and $\omega = \omega_o, \omega_1$) represent the first-order nodal voltage kernels at the microwave LO frequency and IF frequency respectively. The small signal gains of the amplifier were computed from the linear potentials at the 'pump' frequency and the IF frequency. At the microwave frequency the gain of the amplifier agreed within 1-dB in magnitude, over 800 MHz amplifier bandwidth. At the IF frequency the device had a constant gain of 9.2 dB which compares well with the measured gain.

The second-order and all even-order terms of the Taylor series expansion of the device nonlinearities contribute towards the first-order side-bands at $(\omega_o+\omega_1)$ and $(\omega_o-\omega_1)$. It was assumed that the IF and the microwave signals are sufficiently small, and that the contributions from terms higher than second-order can be ignored. The second-order kernels are computed by estimating the second-order nonlinear currents, from the linear kernels and second-order coefficients of the expansion. These nonlinear currents are then considered as input signals. These currents are obtained from

$$\hat{i}_{g_{m_2}}(j\omega_o,j\omega_1) = g_{m_2}(V_{21}(j\omega_o) - V_{31}(j\omega_o))* (V_{21}(j\omega_1) - V_{31}(j\omega_1)) \quad (6.4)$$

$$\hat{i}_{C_{gs_2}}(j\omega_o,j\omega_1) = j(\omega_o+\omega_1)C_{gs_2}(V_{21}(j\omega_o) - V_{31}(j\omega_o))* (V_{21}(j\omega_1) - V_{31}(j\omega_1)) \quad (6.5)$$

$$\hat{i}_{C_{dg_2}}(j\omega_o,j\omega_1) = j(\omega_o+\omega_1)C_{dg_2}(V_{51}(j\omega_o) - V_{21}(j\omega_o))* (V_{51}(j\omega_1) - V_{21}(j\omega_1)) \quad (6.6)$$

where

$$V_{n1}(-j\omega_o) = V^*_{n1}(j\omega_o) \tag{6.7}$$

$$V_{n1}(-j\omega_1) = V^*_{n1}(j\omega_1) \tag{6.8}$$

and the asterisk indicates the complex conjugate. The second-order kernels are obtained by solving

$$[V_{n2}(j\omega_o,j\omega_1)] = [A(j\omega_o,j\omega_1)]^{-1}[I_{2i}(j\omega_o,j\omega_1)] \tag{6.9}$$

where

$$I_{2i}(j\omega_o,j\omega_1) = \begin{bmatrix} 0 \\ -\hat{i}_{C_{gs_2}} + \hat{i}_{C_{dg_2}} \\ \hat{i}_{C_{gs_2}} \\ \hat{i}_{gm_2} \\ \hat{i}_{C_{dg_2}} - \hat{i}_{gm_2} \\ 0 \end{bmatrix} \tag{6.10}$$

These second order kernels were numerically computed at frequencies $\omega_o-\omega_1$, $\omega_o+\omega_1$, ... The numerical values of $Z_L(\omega)$ and $Z_S(\omega)$ were substituted for the frequency of computation, viz. $\omega_o+\omega_1$ for upper side-band and $\omega_o-\omega_1$ for the lower sideband.

6.5 Computation of Up-conversion Characteristics

Two signals at frequencies ω_o and ω_1 are applied at the amplifier input for achieving up-conversion. The input signal may be written in the form

$$v_i(t) = V_1 \cos\omega_o t + V_2 \cos\omega_1 t \tag{6.11}$$

ω_o is the 'pump' frequency and lies in the pass band of the amplifier and ω_1 is the IF frequency. Equation (6.11) may be written in the following form

$$v_i(t) = \frac{1}{2} [V_1 \exp(j\omega_o t) + V_2 \exp(j\omega_1 t) + \text{C.C.}] \tag{6.12}$$

where CC represents the complex conjugate. The inband products are generated at $\omega_o \pm \omega_1$, $\omega_o \pm 2\omega_1$, ... The objective here is to compute the first-order side-band components generated in the output.

The steady state output response at the frequency $\omega_o - \omega_1$ (lower side-band) is given by

$$y_{\omega_o-\omega_1} = \frac{1}{4} [\{V_{o_2}(j\omega_o,-j\omega_1) + V_{o_2}(-j\omega_1,j\omega_o)\}\exp(j(\omega_o-\omega_1)t) + \text{C.C.}] \tag{6.13}$$

$$= \frac{1}{2} [[V_{o_2}(j\omega_o,-j\omega_1)]e^{j(\omega_o-\omega_1)t} + \text{C.C.}] \tag{6.14}$$

Taking only the real parts in the above equation.we get

$$y_{\omega_o-\omega_1} = |V_{o_2}(j\omega_o,-j\omega_1)|\cos[(\omega_o-\omega_1)t + \angle V_{o_2}(j\omega_o,-j\omega_1)] \qquad (6.15)$$

The microwave up-conversion efficiency is defined as the ratio of the up-converted output to the microwave input[83],[84] .

$$\eta = \frac{\text{Sideband (Up-converted) Output}}{\text{Microwave Input}} \qquad (6.16)$$

The up-conversion efficiency in term of the Volterra kernels computed here can therefore be defined as

$$\eta_{dB} = 20\log_{10}\left|\frac{V_{o_2}(j\omega_o,-j\omega_1)}{V_1(j\omega_o)}\right| \qquad (6.17)$$

The above equation gives the lower side-band conversion efficiency. The upper-band conversion efficiency can be obtained by changing the sign of the argument ω_1 in the above equation. From equation (6.17) conversion efficiency was computed as a function of the LO frequency, the IF signal power level and the transistor gate-bias voltage.

6.6 Theoretical and Experimental Results

Experimental results were obtained using the set-up described in Figure 6.1. The MESFET amplifier used an HP HFET-1101 device. The amplifier had a gain of 7.6 dB at 6 GHz and 1-dB bandwidth of 1 GHz at V_{DS}= 3.0V and V_{GS}= -1.0V. The gain of the device at the IF frequency of 70 MHz was 9.2 dB and was observed to be constant for frequencies up to almost 1 GHz. The IF signal was applied using an HP 3200B VHF Oscillator. The microwave pump signal was applied using an HP 8690A sweep oscillator. An HP 8555A Spectrum Analyzer was used at the output of the amplifier to monitor the side-band signal at the output of the device. The IF signal at the input and output of the amplfier was monitored by using a Tektronix 7400 oscilloscope. The behavior of the up-conversion efficiency as a function of IF signal power level is shown in Figure 6.3. The drain-bias was kept at 3 V and the gate-bias was maintained at -1.25 V. It is observed that the theoretically computed results and experimentally measured results agree within 3 dB in magnitude. The conversion efficiency increases by 1-dB for every 1-dB increase in IF signal level. This is to be expected since the mathematical model indicates that the first sideband around the LO frequency comes largely from the second-order terms of the expansion of nonlinear terms. At relatively higher input IF levels (P_{IF} =0 dBm), the measured conversion efficiency tends to saturate because of the limited output power capabilities of the device.

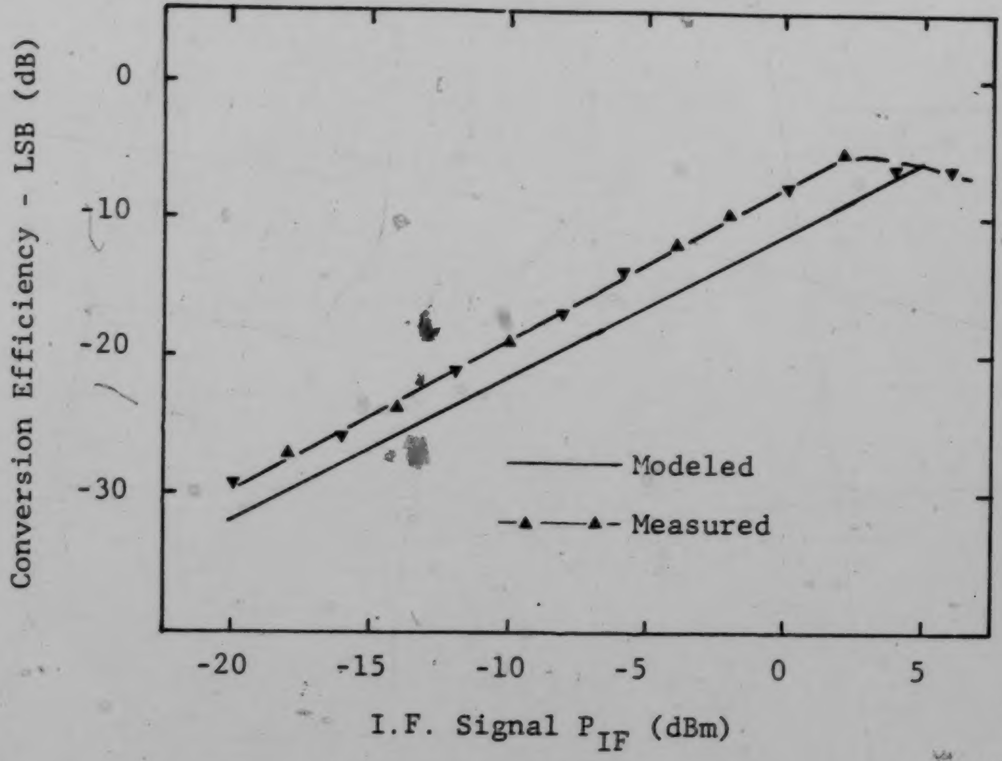


Fig. 6.3 Lower Side-band Up-conversion Efficiency of the MESFET Amplifier as a Function of IF Signal Power Level; Device HP HFET-1101, $V_{DS} = 3.0V$, $V_{GS} = -1.25V$

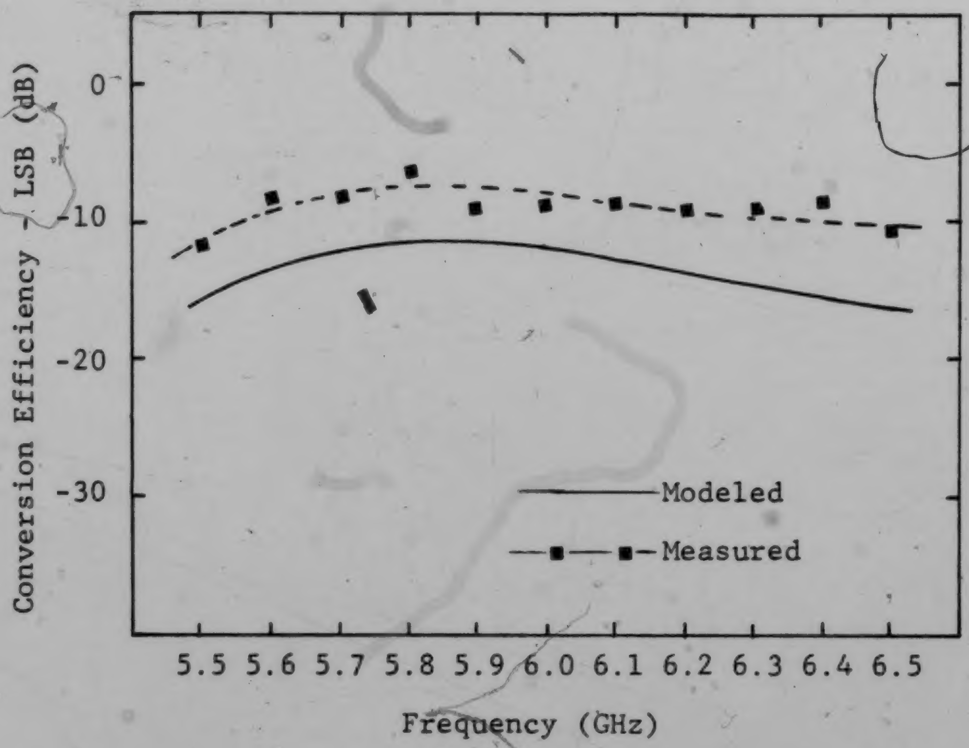


Fig. 6.4 Lower Side-Band Up-Conversion Efficiency of the MESFET Amplifier as a Function of Signal Frequency; Device HP HFET-1101, $V_{DS} = 3.0V$, $V_{GS} = -1.25V$

Figure 6.4 shows the conversion efficiency as a function of the microwave LO frequency. It is quite apparent from the results that the conversion efficiency curve largely follows the amplifier frequency response characteristics. For the large bandwidth amplifier therefore, the bandwidth of the up-converter is also larger. It may be pointed out here that 1 GHz bandwidth is not necessarily required in a practical up-converter. A few MHz of bandwidth is normally sufficient for transmission of information in practical systems. Any attempt to increase the amplifier bandwidth for a given device normally results in a decrease of the associated gain. The experimentally measured results closely follow the theoretically predicted results over 1 GHz bandwith of the amplifier up-converter.

The experimentally measured conversion efficiecy as a function of the transistor gate-bias is shown in Figure 6.5. It is observed that the conversion efficiency is larger at gate-biases near the pinch-off voltage and near the current saturation regime of the device operation. A minimum is observed near V_{GS} =-0.85 V, and the efficiency increases on both sides of this operating point. This is to be expected, since a partial clipping of the microwave LO and the IF signal causes increased conversion efficiency in these regions of increased nonlinearity. This experimental behavior is consistent with the results reported for a GaAs FET frequency-multiplier [7].

The Volterra-series model is inadequate for the

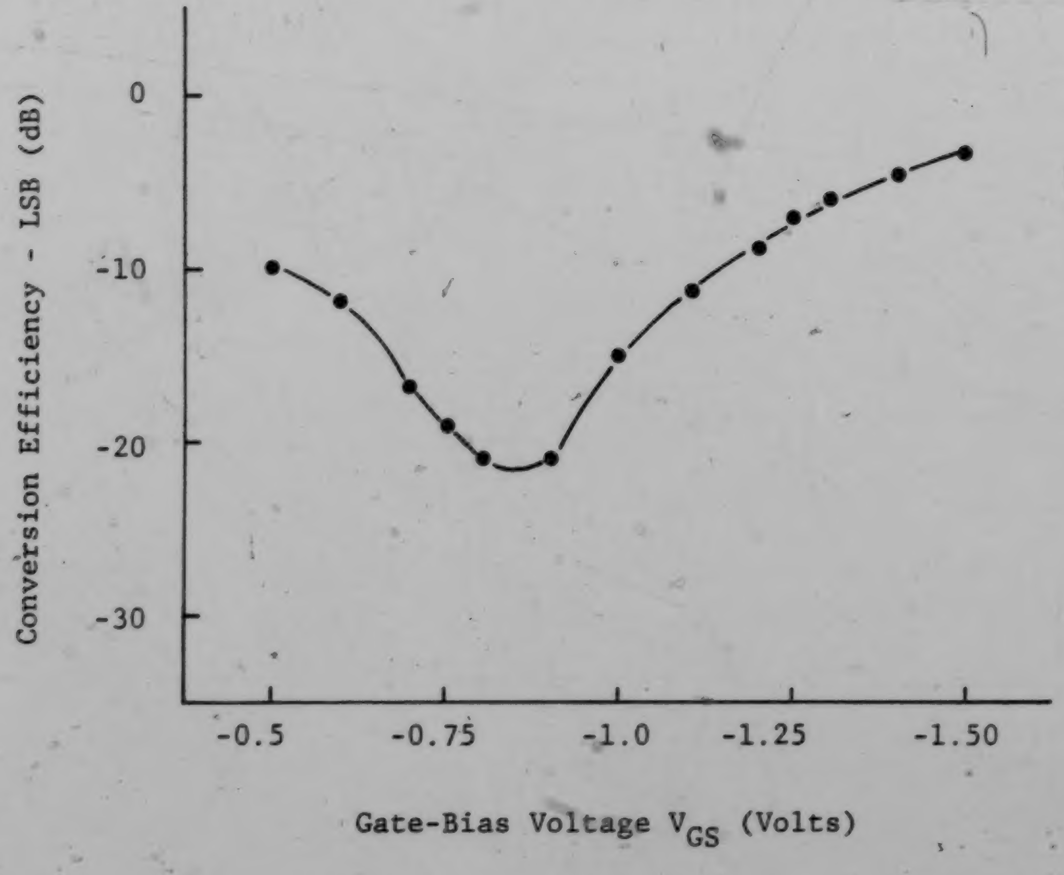


Fig. 6.5 Lower Side-Band Up-Conversion Efficiency of the MESFET Amplifier as a Function of Transistor Gate-Bias V_{GS}; Device HP HFET-1101, V_{DS} = 3.0V

analysis of up-conversion characteristics in the region of increased conversion efficiency. Alternatively, the voltage and current waveforms within the device could be computed in time-domain by using nonlinear system analysis programs. The computation of the waveforms is done by time-domain analysis of device potentials and by modeling their interaction with the circuit in frequency-domain. These waveforms can be Fourier analysed to compute the up-conversion efficiency. Since relatively large nonlinearities can be taken into account, such an analysis should give better predicted values.

CHAPTER VII

SUMMARY, CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER RESEARCH

7.1 Summary

In this thesis, a systematic mathematical approach has been developed for the linear and nonlinear analysis of a GaAs FET amplifier. The following measurement and modeling techniques have been developed during this study:

1) A method has been developed for accurate characterisation of a GaAs FET device. The characterisation technique features: a) the measurement of device S-parameters in the same fixture and under same mounting conditions as used in the final amplifier, b) the use of a network analyzer for fast measurements, c) the use of a CAD program for modeling of the fixture and of the device, d) the de-embedding of the device S-parameters from the microwave circuit, and e) removal of the network analyzer system measurement errors by a computer error correction routine. The accuracy of the measurements is estimated to be approximately 10% for S_{11}, S_{22}, and S_{21}.

2) A 6 GHz integrated microwave amplifier has been realised using microstrip circuits and a GaAs FET device. A distributed model for the GaAs FET amplifier has been proposed. The model allows computation of the magnitude and

phase response at the external ports of the amplifier. The distributed circuit model has been transformed into a generalised lumped circuit model for the GaAs FET amplifier. The proposed model has the advantage of explicitly describing the interaction of the active device with the microwave circuit at all frequencies within the amplifier band. The validity of the model has been demonstrated by comparing the measured and modeled small-signal results over a 1 GHz amplifier bandwidth.

3) A nonlinear model for intermodulation distortion analysis of a GaAs FET amplifier has been developed. The model has been applied for predicting the amplifier output response for an equal amplitude two-tone signal at the amplifier input. This model is based on a Volterra-series representation of the amplifier input/output response. The Volterra-series is particularly suitable for modeling the nonlinear amplifier response, because it allows the memory effects associated with the amplifier response at microwave frequencies to be included in the analysis. In general, the Volterra-series consists of an infinite number of terms. The first few terms are, however, adequate for modeling of the distortion, in the current saturation region of the device.

The computed results for the two-tone intermodulation distortion have been compared with the experimentally measured results. These computations and measurements have been made as a function of parameters extrinsic to the device, such as the microwave input signal level, microwave frequency and the transistor gate bias. At small input signal levels (less than -10 dBm), measured and predicted results agree within 3-dB over a 400 MHz frequency range.

4) A gate-bias compensation technique has been described for improving the intermodulation distortion performance of the GaAs FET amplifier. The technique utilises transistor gate-bias compensation controlled by the input signal level of the amplifier. For a constant power output of 0 dBm an improvement in the third-order intermodulation distortion product of up to 10 dB has been observed. The technique has the advantage that improved distortion performance of the amplifier is obtained for increasing input microwave power levels and it is very simple to implement. The technique is, however, useful only over a limited range of gate-bias.

5) A method has been described for achieving up-conversion in a single-gate MESFET amplifier. A mathematical model has been proposed for analysis of the up-conversion characteristics of the amplifier. The model takes into account the device nonlinearities and their interaction with the impedances seen by the device at the various frequency components which are present at the input and output of the amplifier.

7.2 Conclusions

The following general conclusions can be drawn from the computed and measured results described in this thesis

1) Intermodulation distortion in the low-noise low-power GaAs FET amplifier described in this thesis increases with a 3:1 ratio as a function of the input microwave power level. For most of the microwave amplifiers, such a behaviour should be expected because of large contribution from cubic nonlinearities. For certain power GaAs FETs, the intermodulation distortion is ill-behaved and the concept of intercept point does not hold. It can be concluded that, for low power GaAs FETs, the intermodulation distortion is well behaved in the current saturation region of the device operation and the concept of the intercept point remains valid.

2) The drain-to-gate Miller capacitance makes a significant contribution to the amplifier distortion . Therefore, the nonlinear coefficient associated with the feedback capacitance should not be ignored in the analysis.

3) From the frequency dependence of the intermodulation distortion, it is observed that the distortion is a maximum at the frequency where power transfer from the device to the output microwave circuit is a maximum. For the device under test, the distortion at the frequency of output match is observed to be 4.2 dB more than at the frequency of input match. Therefore, it may be concluded that better distortion

performance can be obtained from an amplifier by detuning the output from the frequency range of interest. Such detuning results in improvement of the distortion at the cost of the amplifier gain.

4) The IM_3 is observed to be a strong function of the device biasing conditions. In the current saturation region of the device under test, the IM_3 is observed to decrease by approximately 6 dB for each -0.25V change in gate-bias. Because of interaction of the device nonlinearities and the device gain, a point of inflection is reached at which the distortion is minimum. This point of minimum distortion was observed to be at a gate-bias of -1.52 V. Beyond this gate-bias IM_3 increases rapidly and there is a large decrease in the amplifier gain.

5) When the device is used as an up-converter, the conversion efficiency curve largely follows the amplifier frequency response characteristics. Therefore, for design of a large bandwidth up-converter the amplifier should also have a large bandwidth.

6) The conversion efficiency increases by 1-dB for every 1-dB increase in IF signal level. At relatively higher input IF levels (P_{IF} = 0 dBm) the measured conversion efficiency tends to saturate because of the limited power capabilities of the device.

7) The measured conversion efficiency is larger at a gate-bias near the pinch-off voltage and near the saturation region of device operation. A minimum has been observed near V_{GS}

=-0.85V. A maximum conversion efficiency of -3 dB was obtained.

8) Volterra series modeling is inadequate for the analysis of the up-conversion efficiency in regions of increased conversion efficiency because of the relatively severe nonlinearities encountered in these regions.

7.3 Recommendations For Further Research:

The mathematical approach described in this thesis can be extended to study the following additional performance characteristics of the GaAs FET amplifier.

1) The analysis can be extended to study the intermodulation distortion as a function of various gate and drain biasing potentials. This information will be useful in theoretically determining the optimum bias conditions for the device. The optimum bias point could then be externally controlled so as to operate the device in the region of lowest intermodulation distortion.

2) In communication systems the devices are normally used in cascade operation to obtain higher gains and power outputs. Since an overall systems approach has been developed, the analysis can be conveniently extended for analysis of intermodulation distortion in devices used in cascade operation.

3) The analysis has demonstrated that the intermodulation distortion is a strong function of the load

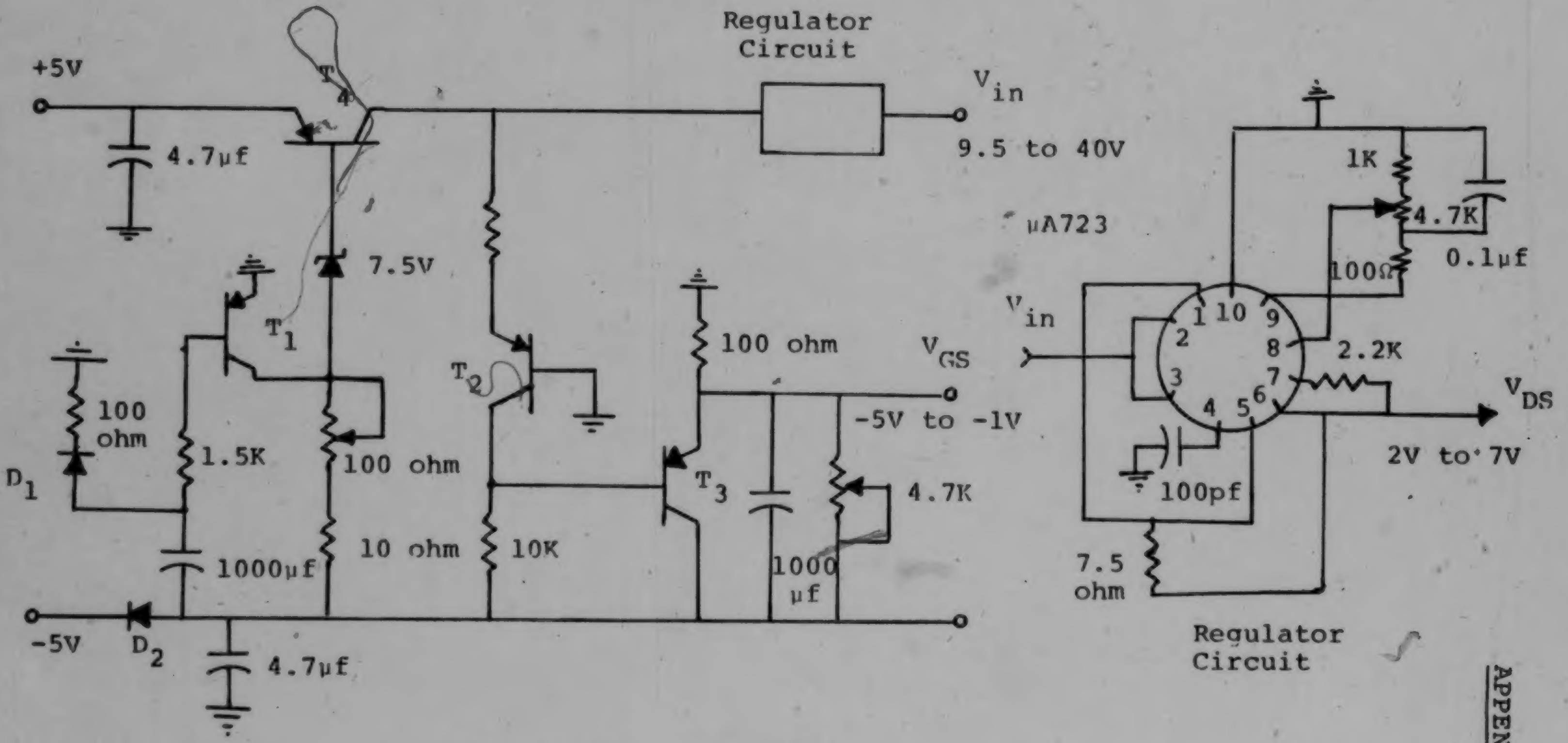
termination. By simple extension of the analysis, the intermodulation distortion can be computed for various load terminations along with constant gain circles at the output. Such information could be helpful in selecting output terminations for optimum gain and distortion trade-offs.

4) The analysis can be further extended to model the amplifier output response for various forms of input signals, such as QPSK microwave signals. Such analyses would be useful for communication system applications of the GaAs FET amplifier.

5) The Volterra-series has been found to be inadequate for predicting the up-conversion characteristics of the amplifier in the regions of maximum up-conversion efficiency. Alternatively, the voltage and current waveforms within the device can be computed in the time-domain by using nonlinear system analysis programs. Since such an analysis would require information about device nonlinearities and the circuit impedances, the measurement techniques developed in this thesis and the nonlinear model can be used for the analysis.

A recapitulation of the results reported in the thesis indicates that almost all the thesis objectives stated in Section 1.2 have been met and that many further extensions are possible. The author hopes that this work will provide a basis for further research work on the performance of GaAs FET amplifiers and their applications in telecommunication systems.

APPENDIX I-A


Regulator Circuit
+5V
4.7µf
T4
7.5V
T1
100 ohm
D1
1.5K
100 ohm
1000µf
10 ohm
-5V
D2
4.7µf
T2
10K
100 ohm
T3
1000 µf
4.7K
VGS
-5V to -1V
Vin
9.5 to 40V
µA723
Vin
1K
4.7K
0.1µf
100Ω
2.2K
VDS
2V to 7V
100pf
7.5 ohm
Regulator Circuit

T_1 to T_3	2N 2907 A
T_4	2N 2904
D_1, D_2	1N 4006

Fig. I-A Protective and Delay Circuit for the GaAs FET Amplifier Power Supply

APPENDIX I-B

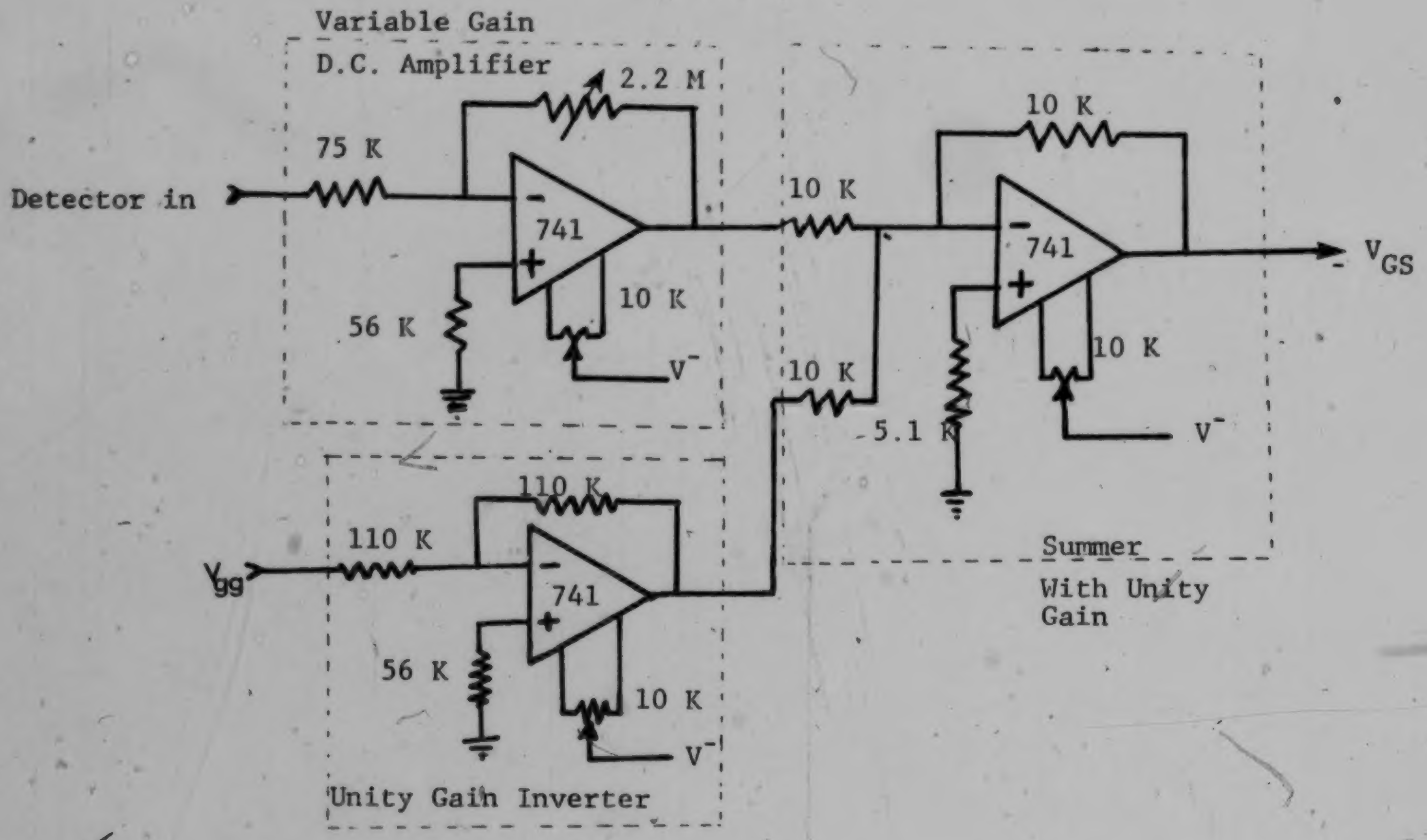

Variable Gain
D.C. Amplifier
2.2 M
75 K
Detector in
741
56 K
10 K
V⁻
10 K
10 K
10 K
741
V_GS
10 K
5.1 K
V⁻
Summer
With Unity
Gain
110 K
110 K
V_gg
741
56 K
10 K
V⁻
Unity Gain Inverter

Fig. I-B D.C. Amplifier for Gate-Bias Compensation of the GaAs FET Amplifier

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